

MODELING AND SCREENING ON-CHIP  
INTERCONNECT INDUCTANCE

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# Abstract

As technology scales, interconnect parasitic effects are becoming increasingly significant, directly limiting circuit performance and wiring density. Post-layout full-chip parasitic resistance and capacitance extraction is now a standard step in VLSI design flow. Due to higher clock frequencies, and lower resistivity copper interconnects, inductance can no longer be neglected in interconnect design. Full-chip inductance extraction is known to be prohibitively complex because of the long-range of inductive coupling and unknown current return paths.

While resistance and capacitance always need to be included in the interconnect model, inductance effects are important only under certain conditions. As a result, it would be a significant waste of resources to include millions of inductance models in design simulations. Because current static timing analysis tools cannot handle inductance and because circuit simulations including inductance are time consuming, a tool is needed to screen and identify nets with significant inductance effects, as well as to estimate the delays of these nets.

First, we study the frequency behavior of current return paths for inductance extraction. From full-wave electromagnetic simulation and delay simulation results, we provide a return path model suitable for full-chip inductance extraction. In the second part, we develop the criteria to identify nets with significant inductance effects.

A two-step inductance screening algorithm is developed based on the inductance effect on signal delay. Parameterized delay models for  $RC$  and  $RLC$  trees are developed to take into account the finite input rise time and resistive shielding. A stand-alone inductance screening tool is implemented based on a standard net parasitic extraction output file and a timing technology library. Applying the screening tool developed in this work to various IC designs shows that less than 0.1% of the nets in a design have inductance problems, supporting the necessity of an inductance screening process before performing inductance extraction. The results show that there is a range of net lengths where inductance effects are significant.

The approach and guidelines provided in this thesis will enable future parasitic extraction and static timing analysis tools to screen and model interconnects with inductance effects.

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# Chapter 1

## Introduction

As anticipated by Moore's law, the number of transistors in an integrated circuits (IC) has doubled every two to three years. The device size and the switching delay have shrunk continuously. Figure 1.1 shows the highest frequency achieved by microprocessors for each technology node. At present, 90 nm technology is in production and microprocessor clock frequencies are above a GHz. The speed of an electrical signal in an IC is governed by two components. The first component is the switching time of an individual transistor, known as transistor gate delay, and the second one is the signal propagation time between transistors, known as wire delay or interconnect delay. Since many generations ago, the device switching speed no longer limits the circuit performance, but the wire delay becomes dominant. To overcome the bottleneck in performance due to on-chip wires, new interconnect technologies such as copper and low-k dielectric materials have been introduced to reduce wire resistance and capacitance [1]. The resistivity of copper is 40% lower than that of aluminum. The dielectric constant of  $\text{SiO}_2$  is 3.9. New materials, such as Fluorinated Silica Glass

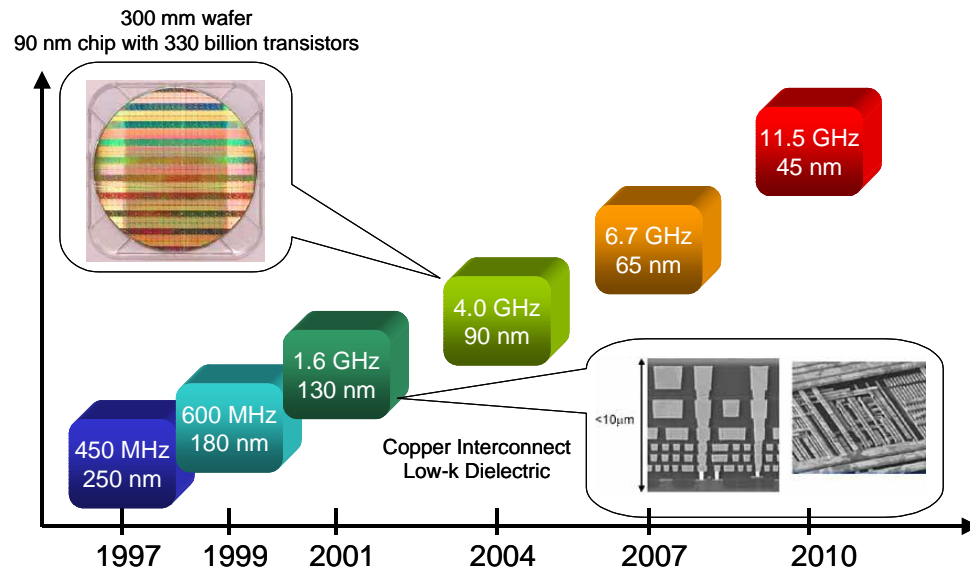


Figure 1.1: VLSI technology scaling. Source: ITRS Roadmap, Intel Corporation.

(FSG) and Black Diamond, have dielectric constants approaching 3.0. Other materials with even lower dielectric constants are being studied extensively. A low dielectric constant reduces the wire delay, capacitive crosstalk noise, and switching power.

## 1.1 VLSI On-Chip Interconnects

Figure 1.2 shows the interconnect lengths at which the wire delay is equal to the gate delay for local, intermediate and global interconnects as predicted in the ITRS roadmap [2]. This figure indicates that, as technology scales, the wire length at which the wire delay starts to dominate becomes shorter. Due to the growing importance of wire delay, circuit designers have been putting increasing efforts on wire design and analysis.

Figure 1.3 shows a typical VLSI CAD flow for full-custom and standard cell design.

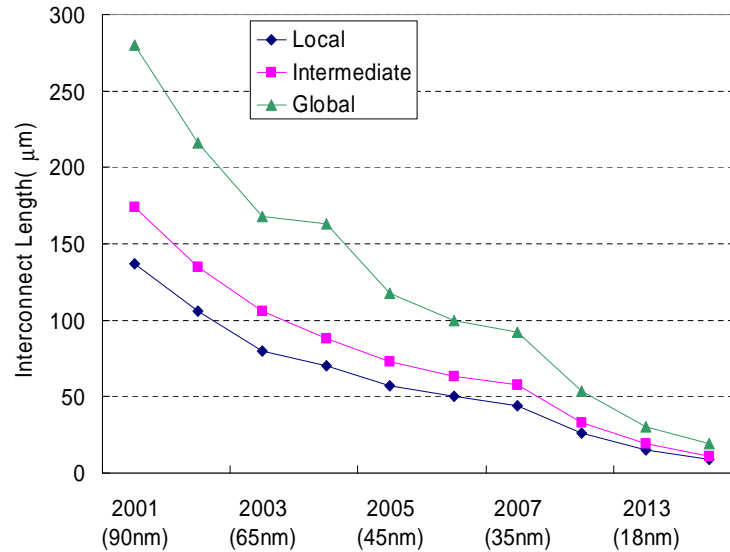


Figure 1.2: Interconnect delay will dominate the total delay for future technologies.

Full-chip interconnect resistance ( $R$ ) and capacitance ( $C$ ) extraction is now a standard step performed after completing the physical design and before performing the timing analysis in the design flow. In full-custom design,  $RC$  extraction is also done during the design stage to take into account the parasitic interconnect effects. In standard cell design, quick interconnect parasitic extraction and delay estimation are done at the place and route stage for optimum placement. Interconnect design is starting to be considered at even earlier stages of the design flow such as gate-level netlist generation. Since the interconnect design affects every stage of the design flow, fast and accurate full-chip level parasitic extraction and delay estimation are becoming increasingly important.

Line parasitics can be accurately extracted using 2-D and 3-D electro-magnetic field-solvers, such as Maxwell and Raphael [3, 4]. However, it is impossible to use

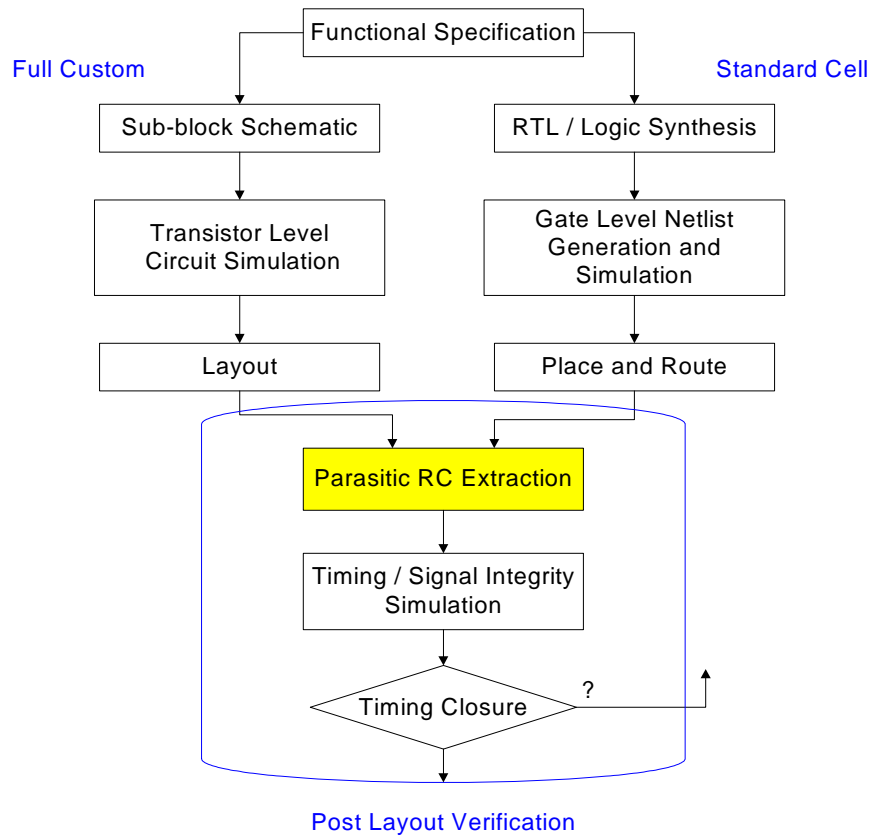


Figure 1.3: Parasitic  $RC$  extraction has become a standard step in VLSI design flow.

these tools at the full-chip level. Currently, full-chip parasitic  $R$  and  $C$  extraction is done, by first building a look-up table for predefined patterns using the field-solvers or experimental test structures. Then the extraction engine performs matching and interpolation between the actual layout and the patterns in the look-up table. For  $R$  and  $C$  extraction, fairly accurate full-chip extraction tools are available from various commercial CAD tool vendors [5, 6, 7].

Because of the higher operational frequencies and lower resistivity copper interconnects, inductive impedance of the on-chip wires become comparable to or larger than the resistive impedance. Therefore, inductance ( $L$ ) can no longer be neglected in interconnect design. Inductance is a physical property of a closed current loop. Inductive coupling can occur over a long distance, whereas capacitive coupling is limited to adjacent interconnects. As a result, it is not straightforward to extend the existing parasitic extraction engine approach to perform inductance extraction.

In a real chip environment, there are multiple potential current return paths, parallel power and ground lines, silicon substrate, or even other signal lines. When the current return path is not known a priori, the *Partial Element Equivalent Circuit* (PEEC) model [8] can be used in principle. However, the PEEC model results in a dense inductance matrix and an unmanageable number of circuit elements [9, 10]. So, sparsifying the inductance matrix is not trivial [11, 12]. As an alternative, *Loop* model is preferred due to its simplicity. In order to apply the loop inductance model for an on-chip interconnect, the current return path needs to be located to define a current loop.

Once the inductance of a net is identified, it is necessary to develop a model to estimate the delay. A typical net in a VLSI design is a tree structure, and the Elmore

delay [13] is the most widely used model due to its closed form formulation and computational efficiency. The model is based on the first moment of the impulse response, which is a single pole approximation of the  $RC$  system. Recently, an equivalent Elmore delay for  $RLC$  trees [14] has been derived from a two pole approximation. The difficulty in  $RLC$  delay model development is the non-monotonic waveform and signal reflection from transmission line effects [15, 16].

There are two major limitations in delay models that are based on Elmore's approximation. First, they do not take into account the input rise time [17]. Second, the models overestimate the delay for near-end nodes (i.e. near the driver or source) [18]. This overestimation comes from the resistive shielding of downstream capacitance. The most common approach to overcome these limitations is to calculate the higher order moments [19, 20]. But this method requires more tree traversals, which considerably reduces the efficiency of the delay models.

Although the significance of inductance is growing, its effects are prominent only under certain conditions for a selected number of nets [21, 22]. Since the total number of nets in a modern IC design can easily exceed millions, including inductance for all the nets in the design is inefficient and unnecessary. Current timing analysis tools do not support the  $RLC$  model, and circuit simulations with inductances are very time consuming.

## 1.2 Organization

In this thesis, we develop a tool to screen and identify nets with significant inductance effects. New  $RC$  and  $RLC$  delay models are proposed to perform screening and to estimate delays of the selected nets.

In Chapter 2, we provide an overview of on-chip interconnect and inductance modeling. As a current return path is necessary to determine the loop inductance, we study the various assumptions and develop analytical formulae that predict the worst case self inductance. By performing full-wave simulations,  $S$ -parameter extraction, and delay simulations, the size of inductance extraction window for accurate inductance extraction is determined. The effect of inter-line capacitors on the current return and inductance extraction is studied as well.

In Chapter 3, we study the inductance effects on signal integrity and discuss when such effects are significant. We present a two-step inductance screening algorithm and a tool to identify the nets which are susceptible to inductance related problem.

New parameterized  $RC$  and  $RLC$  delay models considering the input rise time and resistance shielding of downstream capacitance are presented in Chapter 4. The sensitivity of  $RLC$  delay to inductance is derived based on the proposed delay models.

Chapter 5 shows the inductance screening results of test chips. The results are compared with the theoretical predictions. For the selected nets, several design guidelines are proposed to reduce the inductance effects.

Conclusions are shown in Chapter 6. We also propose future directions on parasitic inductance extraction based on the results presented in this work.

## Chapter 2

# Inductance Modeling

In this chapter, first we review the history of on-chip interconnect models. At the early stage of IC design, all the wires that interconnect the devices were treated as short circuits or lumped capacitors due to the dominance of gate delay. As the wire cross-section dimensions become smaller due to technology scaling, and as the wire length increases, not only the capacitance but also the resistance of the wire becomes significant. In this regime, a wire can be modeled as a lumped resistor and a lumped capacitor when the signal rise time,  $t_r$ , is larger than the one-way signal propagation time through the signal path,  $t_d$ . To improve accuracy as the signal rise time becomes smaller, the wires are modeled as distributed  $RC$  segments as in Figure 2.1. Distributed  $RC$  wire models are necessary when  $t_r/t_d < 2.5$  [23]. Most of the interconnects are modeled as distributed  $RC$  lines in today's designs.

As a solution to curb the increase in  $RC$  delay resulting from the wire scaling and the increase in chip size, multilevel interconnections and copper technology have been introduced [1]. With faster circuit speed and relatively lower resistance from the new technologies, the wire inductance becomes important as well. Figure 2.2 shows

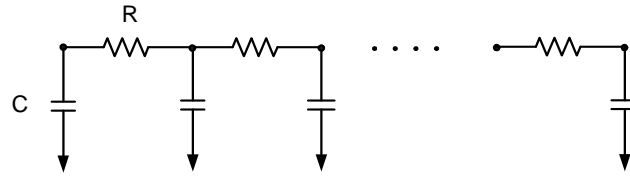


Figure 2.1: An interconnect is modeled as a distributed  $RC$  line.

the resistance ( $R$ ) and inductive part of the line impedance ( $\omega L$ ) as a function of frequency for a given line structure.  $\omega L$  increases drastically as frequency increases.

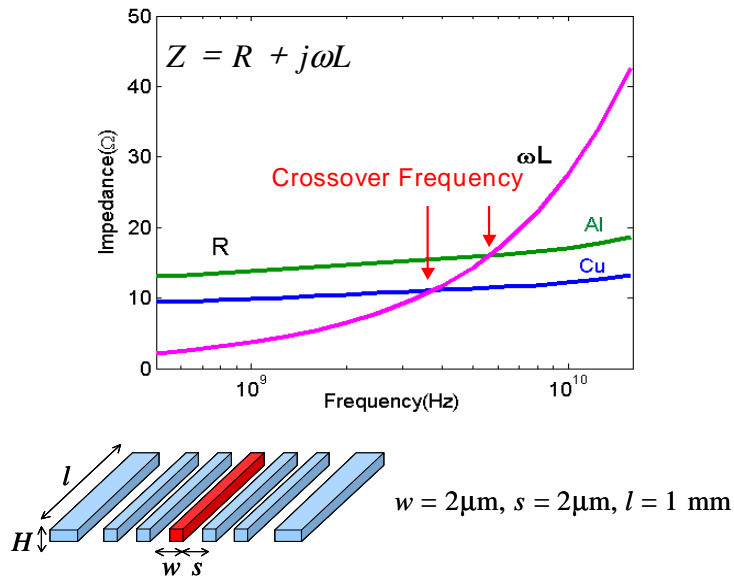


Figure 2.2: As frequency increases, the inductive part of the line impedance becomes comparable to the resistive part.

The resistivity of copper is 40% lower than that of aluminum. Smaller  $R$  further lowers the crossover frequency, and makes inductance effects more likely to occur. When  $\omega L$  becomes comparable to or larger than  $R$ , the wires should be modeled as distributed  $RLC$  lines as shown in Figure 2.3.

Off-chip wires are often approximated as lossless  $LC$  transmission lines due to the relaxed dimensions [24]. However, the resistance of the on-chip wires is not negligible.

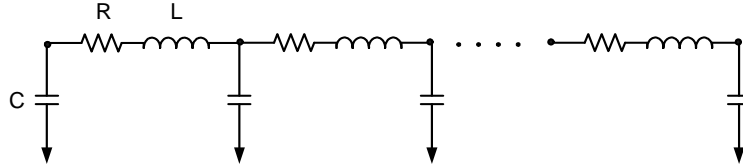


Figure 2.3: An interconnect is modeled as a distributed  $RLC$  transmission line.

So when inductance becomes significant, the on-chip wires should be modeled as lossy  $RLC$  transmission lines. The criterion to select the minimal number of distributed  $RLC$  segments to represent a lossy transmission line is determined from the condition that the propagation delay of an elementary cell should not be larger than one fifth the shortest rise time expected [25]. This condition is expressed as the following:

$$N \geq 5 \frac{d\sqrt{LC}}{t_r} \quad (2.1)$$

where  $d$  is the length of the line,  $C$  is the capacitance per unit length,  $L$  is the inductance per unit length, and  $t_r$  is 10% to 90% signal rise time.

In this chapter, we review the definition, modeling, and extraction of on-chip interconnect inductance. We examine the accuracy of the current return path assumptions in the loop inductance extraction. Analytical formulae are developed to predict the worst case self inductance. In order to determine the inductance extraction window size, full-wave simulations and delay simulations are performed.

## 2.1 Inductance Definition

In this section, we review the governing equations for the magnetic inductance and the interaction between the magnetic and electric fields to derive the definition of

inductance.

A wire carrying an electric current or a time varying electric field creates magnetic fields. This relationship is represented by Ampère's law [23] as the following:

$$\nabla \times B = \mu J + \mu\epsilon \frac{\partial E}{\partial t} \quad (2.2)$$

where  $\mu$  is the magnetic permeability and  $\epsilon$  is the electric permittivity of the material. The first term on the right-hand side represents a magnetic field generated from a wire carrying an electric current. The second term corresponds to the magnetic field generated from the displacement current, which represents the ac current flowing between two conductors due to their capacitive coupling as shown in Figure 2.4. In integrated circuits, the second term is usually neglected because the current flowing in the conductor is much larger than the displacement current [10]. This assumption is called the *magnetoquasistatic* approximation. The accuracy of this assumption will be examined later in this chapter. The integral form of Ampère's law based on Stokes' law is the following:

$$\oint_C B \cdot dl = \mu \int_S \left( J + \epsilon \frac{\partial E}{\partial t} \right) \cdot ds \quad (2.3)$$

where  $C$  is the contour that encloses the surface  $S$ .

Faraday's law states that a time varying magnetic field creates an induced electric field, which is represented as follows:

$$\nabla \times E = -\frac{\partial B}{\partial t} \quad (2.4)$$

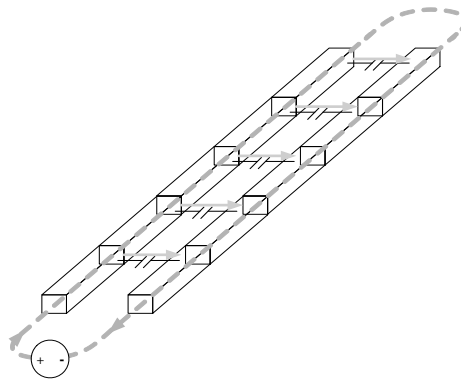


Figure 2.4: Return current through capacitors.

The integral formulation of Faraday's law is the following:

$$\oint_C E \cdot dl = - \frac{\partial \int_S B \cdot ds}{\partial t} \quad (2.5)$$

We can characterize the interaction between electric field and magnetic field from Ampère's law and Faraday's law and derive the expression for inductance. Inductance is a property of the physical layout of a conductor and is a measure of the ability of a conductor configuration to link magnetic flux. The flux linkage is the total magnetic field enclosed by a closed circuit.

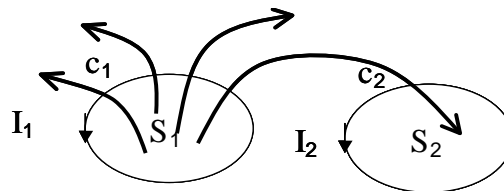


Figure 2.5: Two magnetically coupled circuits.

For two current loops in Figure 2.5, the magnetic flux produced by current  $I_1$  is linked inside the area  $S_2$  which is enclosed by  $C_2$ . The flux linkage enclosed in  $C_2$  is

the following:

$$\Psi_{12} = \int_{\tilde{S}_2} B_1 \cdot ds_2 \quad (2.6)$$

If the  $C_1$  consists of multiple turns  $N_1$ , the total flux produced is  $N_1$  times larger,  $\Lambda_{12} = N_1\Psi_{12}$ . The *mutual inductance*,  $M_{12}$ , between two loops is defined as the following:

$$M_{12} \equiv \frac{N_2\Lambda_{12}}{I_1} = \frac{N_1N_2\Psi_{12}}{I_1} \quad (2.7)$$

The *self inductance*,  $L_{11}$ , is defined from the magnetic flux produced by  $I_1$  enclosed by the contour  $C_1$  as the following:

$$L_{11} \equiv \frac{N_1\Lambda_{11}}{I_1} = \frac{N_1^2\Psi_{11}}{I_1} \quad (2.8)$$

The magnetic field,  $B$ , is determined from Ampère's law, Equation 2.2. Inductance is defined from the magnetic flux linkage,  $\Psi$ , which is the total  $B$  enclosed in a current loop. In the integral formulation of Faraday's law in Equation 2.5,  $\oint_C E \cdot dl$  corresponds to the voltage drop,  $\Delta V$ , generated from the time varying magnetic field. From the definition of inductance, the voltage drop from a time varying current is the following:

$$\Delta V = -L \frac{dI}{dt} \quad (2.9)$$

## 2.2 High Frequency Effects

As frequency increases, the current distribution inside the conductor changes. These changes are called the skin and proximity effects, and they cause variations in resistance and inductance values.

### 2.2.1 Proximity Effect

If multiple power and ground lines are present near a signal line, the return currents are frequency dependent. Figure 2.6 shows the return current path change when there are multiple power and ground lines present near a signal line. At low frequencies,

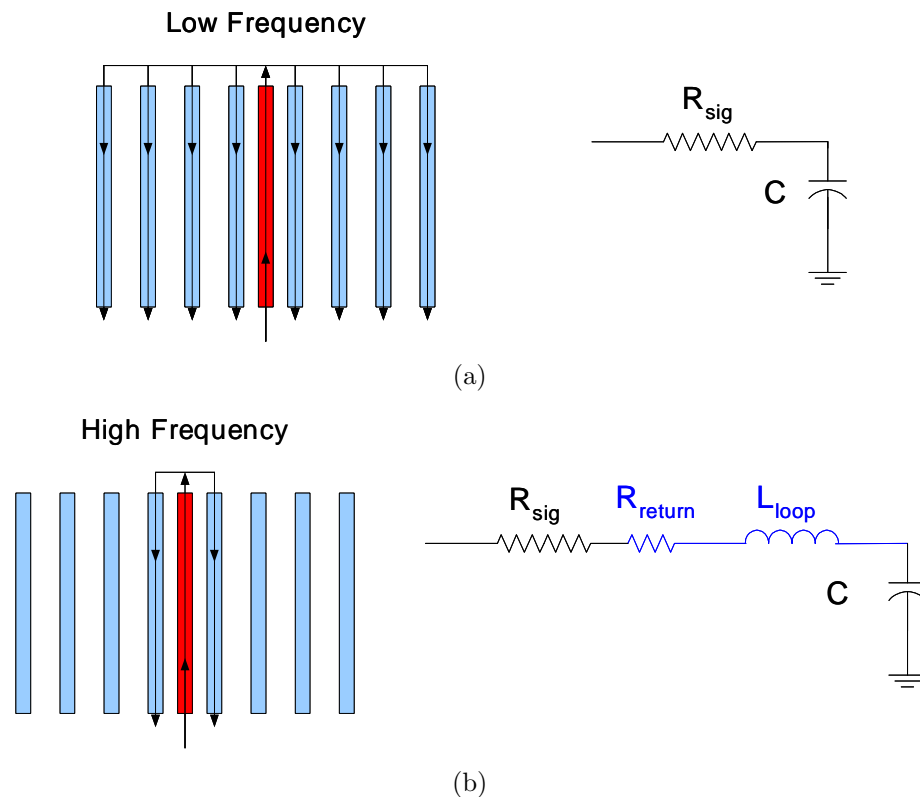


Figure 2.6: Frequency dependent current return path and the interconnect model at (a) low frequency, and (b) high frequency.

the return current is widely spread over multiple wires to minimize the resistance as shown in Figure 2.6(a). At higher frequencies, the return current redistributes to reduce the current loop size to minimize the inductance. Accordingly, at sufficiently high frequencies, the return current flows only through the closest pair of power or ground lines on both sides of the signal line as shown in Figure 2.6(b). It shows

that the high frequency wire model must include the decrease in inductance and the increase in return path resistance due to the narrowing of the return current path. This frequency dependent current return path is called the proximity effect and results in frequency dependent loop resistance and inductance as shown in Figure 2.7 [26]. At higher frequencies, the resistance increases from the return path resistance increase, and the inductance decreases from the shrink in current loop size.

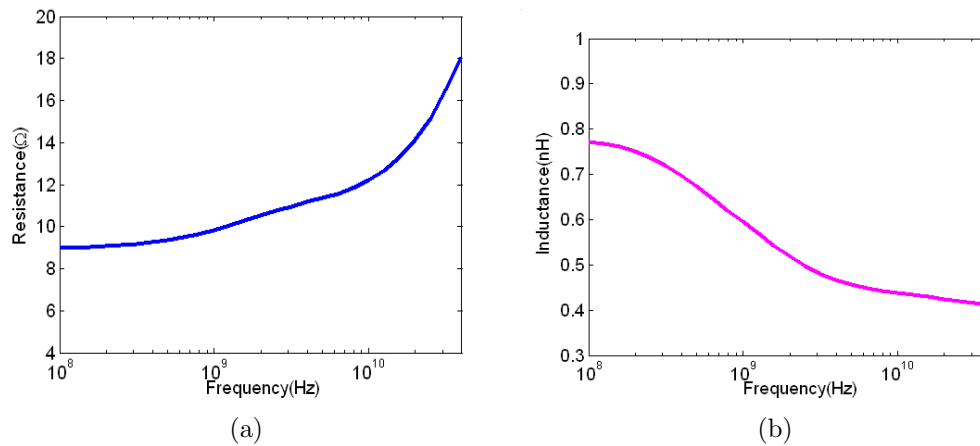


Figure 2.7: Frequency dependent (a) resistance and (b) inductance.

The proximity effect also refers to the current redistribution caused by the magnetic field generated by the neighboring lines [27]. For even-mode coupling, when the current in two neighboring conductors flows in the same direction, the current distribution is concentrated at the far edge of the conductors. For odd-mode coupling, when the current flows in the opposite direction, the current density is higher at the near edge. The current redistribution from the even and odd mode coupling is shown in Figure 2.8.



Figure 2.8: Proximity effect from the current flowing in the neighboring lines. (a) Even-mode coupling. (b) Odd-mode coupling.

### 2.2.2 Skin Effect

The skin effect results in an the exponential increase of the current concentration near the conductor surface as the frequency increases [27]. The total magnetic flux generated by a current can be partitioned into the portion lying outside the conductor plus the flux that lies inside the conductor. The storage of energy associated with the internal flux leads to *internal inductance* and that associated with the external flux is represented by *external inductance* [23]. At high frequencies, the skin effect causes the current to be concentrated near the surface, so the *internal inductance* decreases. As a result, the total inductance decreases and the resistance increases.

The skin depth,  $\delta$ , is defined as the depth at which the wave is attenuated to  $1/e$  (36.8%) of the surface intensity. The skin depth is a function of frequency,  $f$ , magnetic permeability,  $\mu$ , and conductivity,  $\sigma$ , and it is expressed as the following:

$$\delta = \frac{1}{\sqrt{\pi f \mu \sigma}} \quad (2.10)$$

At 1 GHz, the skin depths are  $2.58 \mu\text{m}$  and  $2.09 \mu\text{m}$  for aluminum and copper respectively. At 10 GHz, they become  $0.82 \mu\text{m}$  and  $0.66 \mu\text{m}$  respectively. The skin effect affects the resistance and inductance, only when the thickness and width of the wire are larger than  $2\delta$ . The skin effect effectively reduces the thickness and width of the wires. Since on-chip interconnects are usually designed with minimum

pitch and the analytical inductance formulation has a logarithmic dependence on wire geometries [28], the inductance variation from the skin effect is usually minor. Most of the frequency dependence of on-chip inductance comes not from the skin effect but from the proximity effect. While it is important to consider skin effects when modeling frequency dependent resistance, it is less important when modeling inductance.

### 2.3 Loop and Partial Inductance Models

Inductance is a physical property of a closed current loop. The loop model includes the current return path information in a single inductor and resistor. Figure 2.10(a) shows how a coplanar structure shown in Figure 2.9 is modeled in the loop model. In the loop model, the current return path needs to be determined. However, in a real chip environment, there are multiple return paths available, so it is complex to define a closed current loop. Since the current return path is frequency dependent due to the proximity effect as explained in the previous section, the loop inductance and resistance model are also frequency dependent.

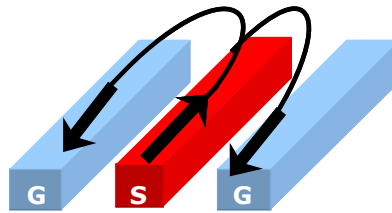


Figure 2.9: Signal line with coplanar current return paths.

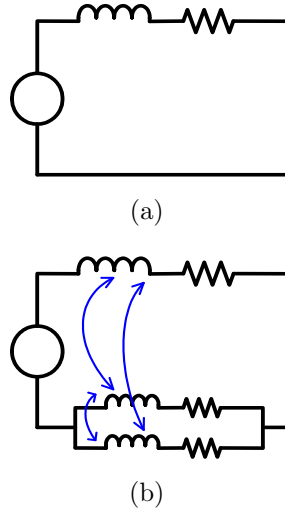


Figure 2.10: The two inductance models. (a) Loop model. (b) PEEC model.

When the current return path is not known a priori, the *Partial Element Equivalent Circuit* (PEEC) model [8] can be used. In the PEEC model, partial self-inductance for each wire segment and mutual inductance between segments are determined. Figure 2.10(b) shows how a coplanar structure shown in Figure 2.9 is modeled using the PEEC model. This fully coupled partial  $RLC$  model is put into a circuit simulator to determine the current return path. In practice, the PEEC model results in an unmanageable number of circuit elements, a dense inductance matrix and excessive simulation time [9]. Hence, the loop inductance model is preferred for full-chip inductance extraction.

In this thesis, we are developing inductance modeling and screening methodologies that are appropriate for full-chip level extraction. Hence the focus is on developing and verifying the methodologies of the loop inductance model.

## 2.4 Inductance Extraction Methods

The most accurate way of extracting inductance is to divide the structure into smaller regions and numerically solve the magnetic field within each region to find the magnetic flux. The HFSS (High Frequency Structure Simulator) from Ansoft [29] is a full-wave 3-D electromagnetic solver based on finite element method optimized for high frequency applications. Although this is an accurate method to extract inductance, full-wave solvers require a large memory and very long simulation time.

FASTHENRY is a fast 3-D inductance extraction tool developed at MIT [30]. FASTHENRY is based on the PEEC modeling of the conductor structure and the *magnetoquasistatic* assumption which is explained earlier in this chapter. To simulate skin and proximity effects, the cross section of each conductor is divided into multiple filaments as shown in Figure 2.11. Mesh analysis is used to reformulate the  $RL$  equations and the dense system of equations are solved iteratively using multipole-accelerated GMRES (Generalized Minimal RESidual) method.

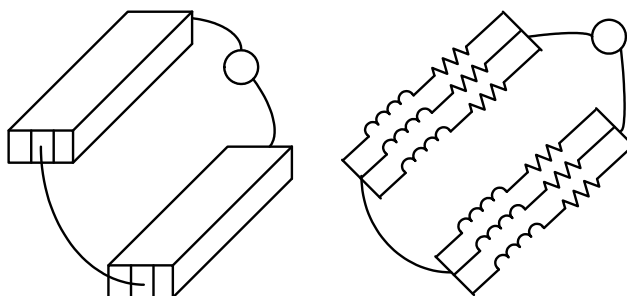


Figure 2.11: Conductors are divided into multiple filaments in the PEEC modeling.

## 2.5 Current Return Path Assumptions for On-Chip Loop Inductance Extraction

In this section, we examine the accuracy of the generally accepted current return path assumption for on-chip loop inductance extraction and propose an improved model with better accuracy. In off-chip interconnects, the current return path is usually well defined, since the return current typically flows to the power/ground plane or to the substrate [24]. In an on-chip environment, there are multiple potential current return paths, such as parallel power and ground lines, the silicon substrate, or even other signal lines. We will not consider other signal lines, because whether a signal line can act as a current return path depends on its switching state, which cannot be determined at the parasitic extraction stage.

### 2.5.1 Analytical Inductance Formulation in the Presence of Multiple Return Paths

The most common assumption, regardless of the frequency of interest, is to restrict the current return paths to the closest pair of power and/or ground [31, 11, 32]. We will call this model the *2-Return Model* as shown in Figure 2.12. This assumption is widely accepted because it localizes the extraction window and simplifies the inductance extraction at the design stage. The model including up to the second neighboring pair will be called the *4-Return Model*.

Figure 2.13 shows the FASTHENRY simulation of loop inductance with different numbers of current return paths as a function of frequency. In this plot, the low frequency inductance values for various return models hold up to around 1 GHz

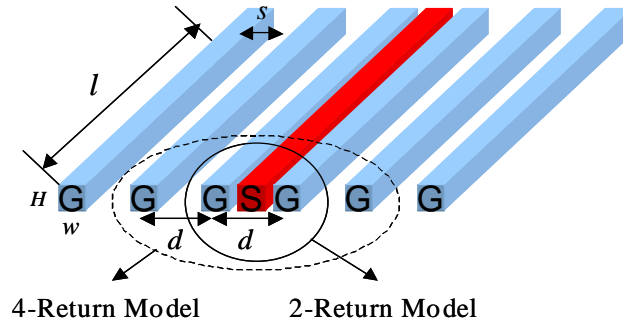


Figure 2.12: Inductance extraction window.

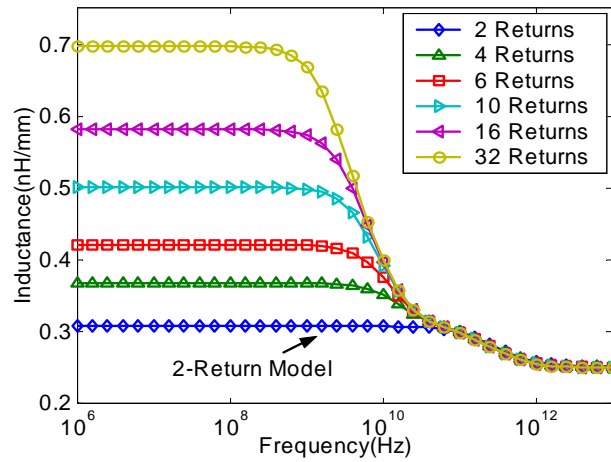


Figure 2.13: Inductance vs. frequency for signal lines with different number of return paths.

before they start to decay, but do not approach that of the *2-Return Model* until 40 GHz. Thus, for frequencies in several GHz range, the *2-Return Model* significantly underestimates the inductance. In order to evaluate the underestimation of the *2-Return Model*, analytical formulae are derived for the worst case loop inductance of a signal line with multiple return paths.

Figure 2.14 shows the return current direction and distribution of a signal line with multiple return paths.

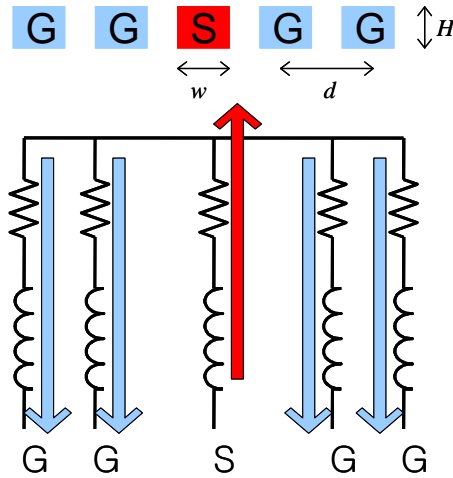


Figure 2.14: Signal line with multiple current return paths.

From energy conservation, the expression of loop inductance can be represented by a weighted sum of partial self and mutual inductance values as the following [33]:

$$L_{Loop} = \sum_i \alpha_i \sum_j \alpha_j L_{ij} \quad (2.11)$$

where the weights,  $\alpha$ 's are calculated from the distribution of the return current which is determined from the return path resistance.  $L_{ij}$ 's correspond to the partial self and

mutual inductances.

$$\begin{cases} \alpha_0 = 1 & (i = 0) \\ \alpha_i = -\frac{R_{GND}}{R_{gi}} & (i > 0) \end{cases} \quad (2.12)$$

$$\begin{cases} L_{ij} = L_{self} & (i = j) \\ L_{ij} = M & (i \neq j) \end{cases} \quad (2.13)$$

Partial inductances,  $L_{self}$  and  $M$ , for rectangular cross section conductors are calculated from the following equations [28].

$$L_{self} = \frac{\mu_0 l}{2\pi} \left[ \log \left( \frac{2l}{w+H} \right) + \frac{1}{2} \right] \quad (2.14)$$

$$M = \frac{\mu_0 l}{2\pi} \left[ \log \left( \frac{2l}{d} \right) + \frac{d}{l} - 1 \right] \quad (2.15)$$

where  $l$  is the line length,  $d$  is the center-to-center distance between conductors,  $w$  and  $H$  are the conductor width and thickness respectively. These equations hold when  $l \gg w, H$ .

The analytical expressions are derived for the worst case loop inductance of a signal line with multiple return paths as shown in Figure 2.15(a) and (b). In order to understand how the worst case loop inductance behaves as a function of the number of possible return paths and geometries, the equations were further simplified in a closed analytical form. Based on the observation that the inductance increase as a function of the number of return paths has a logarithmic trend, the exact analytical formulae are fitted by solving the non-linear least square problem using the Nelder-Mead simplex optimizer [34]. The analytical formulae are the following:

$$L_{sym} = \frac{\mu l}{2\pi} \left[ \left( 1 + \frac{1}{N} \right) \log(2g) - \frac{1}{3} \left( 5N + \frac{2}{N} \right) \left( \frac{d}{l} \right) + 1.02 \log(N + 1.7) - 0.5 \right] \quad (2.16)$$

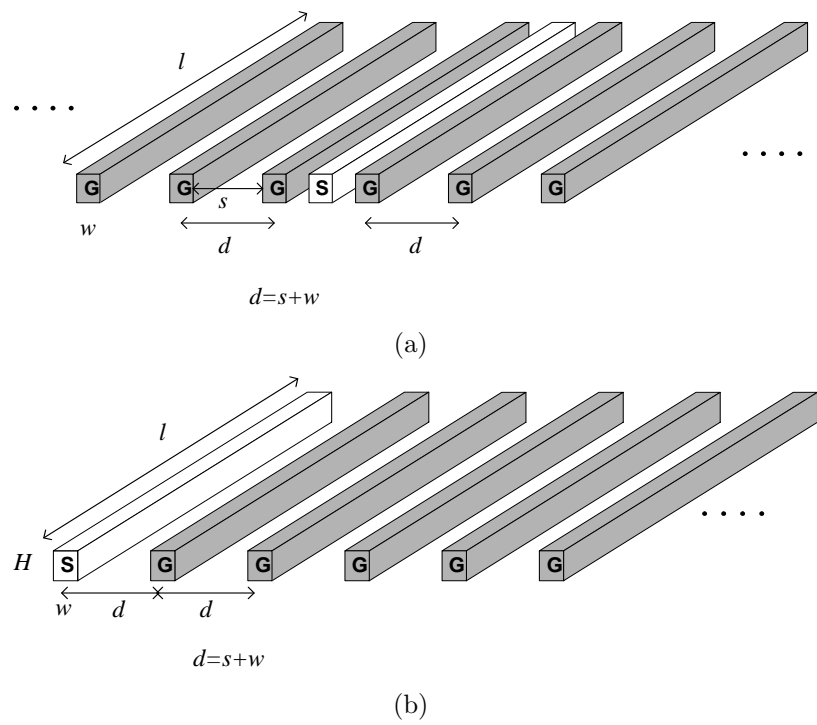


Figure 2.15: Signal line with multiple current return paths. (a) Return paths on both sides. (b) Return paths on one side.

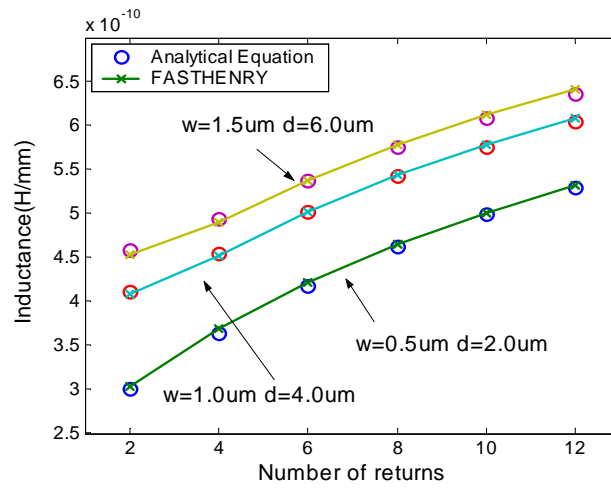
$$L_{one} = \frac{\mu l}{2\pi} \left[ \left(1 + \frac{1}{N}\right) \log(g) - \left(1 + \frac{1}{3N} + \frac{2N}{3}\right) \left(\frac{d}{2l}\right) + 1.06 \log(N + 5.3) + 0.8 \right] \quad (2.17)$$

where

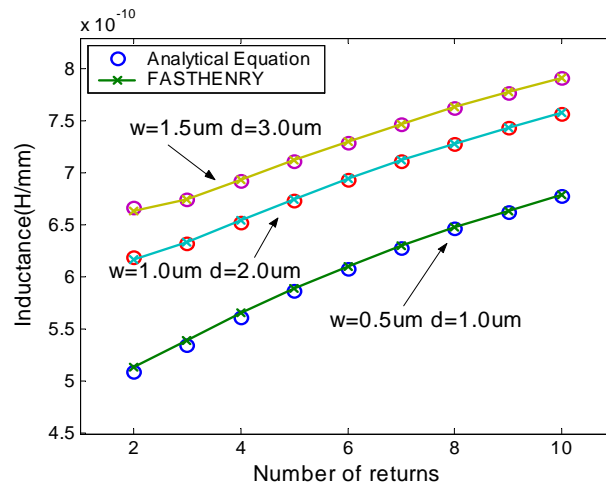
$$g = \left( \frac{d}{w + H} \right)$$

$N$  is the number of adjacent power-ground lines,  $d$  is the center-to-center distance between conductors,  $w$  and  $H$  are width and thickness of return wires respectively. Equation 2.16 is for the signal line with return paths on both sides as in Figure 2.15(a). Equation 2.17 is for the signal line with multiple return paths only on one side as in Figure 2.15(b). Figure 2.16 shows how the low frequency inductance values found from the proposed formula match with those from FASTHENRY.

The geometric dependence of inductance underestimation can be found from the proposed analytical formulae. As  $N$ , the number of return paths, increases, the first term decreases slowly and the third term logarithmically increases. For sufficiently long lines, when  $l$  is much larger than  $d$ , the second term from the formula can be neglected. Only the first term which is characterized with  $g$  has geometric dependence. For small  $g$ , in other words, when spacing between the wires are comparable to wire width, the third term in the formula is dominant, and the underestimation of inductance from the *2-Return Model* is worse. The accuracy improves as  $g$  becomes larger. If  $g$  is sufficiently large, the first term dominates over the third term. Since the first term decreases as  $N$  increases, the underestimation of inductance is negligible. The inductance underestimation in the *2-Return Model* gets worse for smaller  $g$ 's. Parallel signal buses or shielded clock lines are usually closely spaced, and so they have small  $g$ . So, the inductance extraction based on the *2-Return Model* for those lines can generate a large error. Figure 2.17 shows the prediction of geometric dependence



(a)



(b)

Figure 2.16: Accuracy of the analytical formulation for low frequency inductance with return paths on (a) both sides, and (b) one side.

using the proposed inductance model for different  $g$ 's.

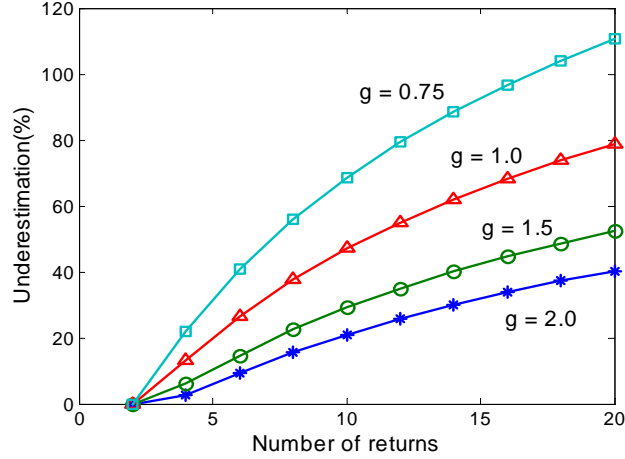


Figure 2.17: Geometric dependence of low frequency inductance underestimation of the *2-Return Model*.

The change in inductance as a function of frequency can be modeled with the Foster network [35] shown in Figure 2.18(a). At low frequencies, inductors have low impedance, so the current flows through  $L_1$  and the total inductance  $L_0 + L_1$ . As frequency increases, more of the total current flows through  $R_1$  and the total inductance approaches  $L_0$ . The values of the circuit elements,  $R_1$ ,  $R_0$ ,  $L_0$  and  $L_1$  are calculated from low and high frequency inductance and resistance values as the following:

$$\begin{aligned}
 R_1 &= R_{HF} - R_{LF} \\
 R_0 &= R_{LF} \\
 L_0 &= L_{HF} \\
 L_1 &= L_{LF} - L_{HF}.
 \end{aligned}
 \tag{2.18}$$

Low frequency inductance,  $L_{LF}$ , can be found from Equation 2.16 or 2.17. Neglecting the skin effect, the high frequency inductance value,  $L_{HF}$ , is found by setting

the current return path only to the closest ones, i.e.  $N = 2$  in Equation 2.16 and  $N = 1$  in Equation 2.17. Figure 2.18(b) shows how our inductance equation combined with the Foster network matches the frequency dependency of inductance.

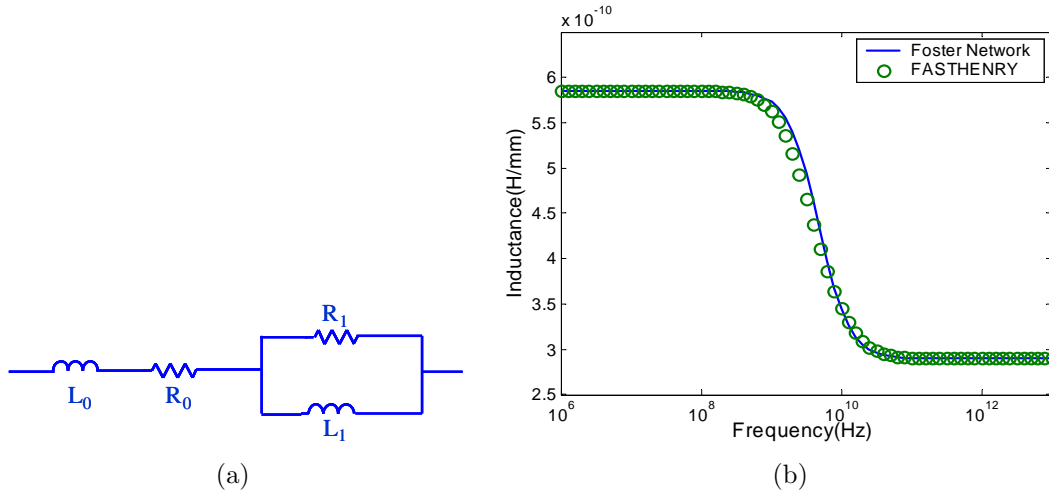
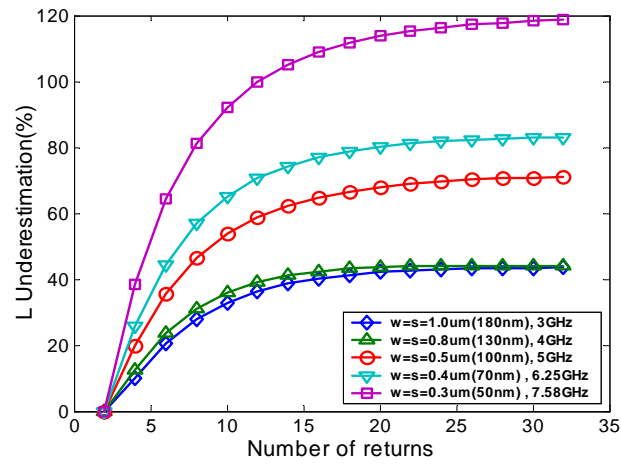
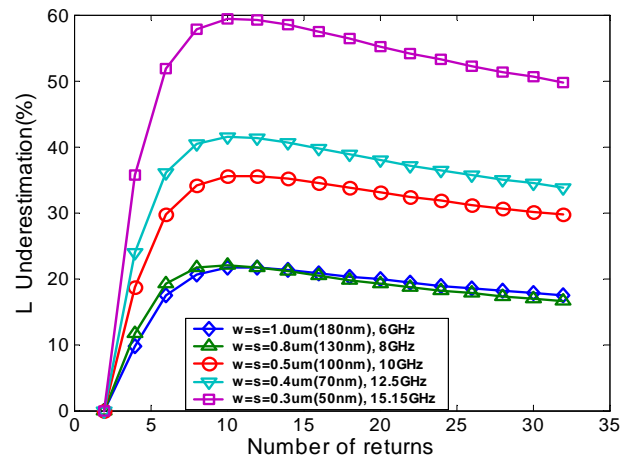


Figure 2.18: Foster network captures the frequency dependence. (a) Foster network. (b) Foster network and FASTHENRY comparison.

The ITRS roadmap predicts the scaling of wire pitch and the signal rise time. Inductance extraction frequency also needs to increase because of the faster signal rise time. Figure 2.19 shows the inductance underestimation of the *2-Return Model* for future technologies calculated from the inductance formulation combined with the Foster network that models the frequency scaling. As technology scales, wire thickness does not scale as fast as wire width and spacing. In Figure 2.19(a), the extraction frequency is set to half of the microprocessor frequency predicted from the roadmap. We can see that due to the scaling of wire pitch, inductance underestimation using the *2-Return Model* will deteriorate further. When the extraction frequency approaches that of the microprocessor frequency as in Figure 2.19(b), the error in the *2-Return Model* becomes less severe. The number of return paths that should be included in



(a)



(b)

Figure 2.19: Inductance underestimation predictions for future technologies based on ITRS roadmap. (a) Clock frequency is half the microprocessor frequency predicted by ITRS. (b) Clock frequency is the microprocessor frequency predicted by ITRS.

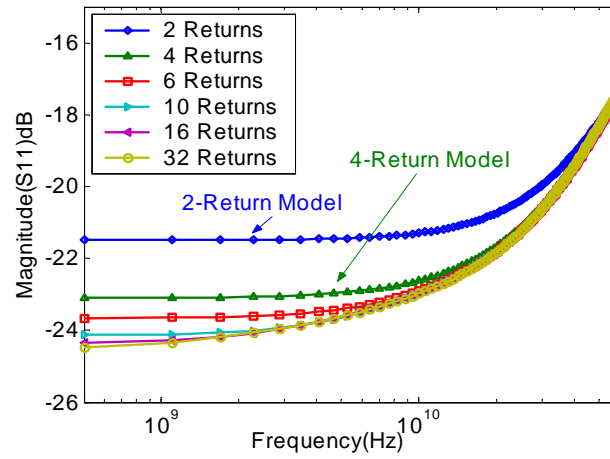
the inductance extraction is a complicated function of wire geometry and operating frequency. Hence, future CAD tools must have the capability to determine the number of return paths that are included in the inductance extraction.

### 2.5.2 Inductance Extraction Window

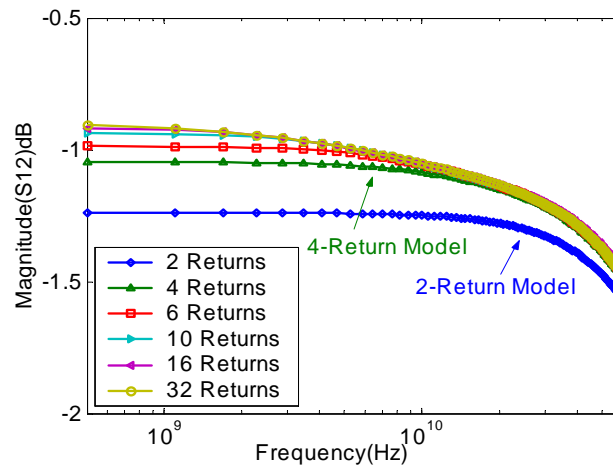
In the previous subsection, it is shown that by including only the closest current return path in the inductance extraction, there can be a significant error in the estimation. In order to examine the effect of frequency dependent return path on actual signal propagation,  $S$ -parameters were extracted using a full-wave field solver (HFSS) [29].  $S$ -parameter characterization shows the actual wave reflection and transport characteristics at the input and output ports.

Figure 2.20 shows the  $S$ -parameter extraction results for a signal line with different number of return paths. The  $S$ -parameters converge to those of the *2-Return Model* at sufficiently high frequencies. Throughout most of the frequency range, the  $S$ -parameters do not change much by including more than 4 return lines.

Figure 2.21 shows delay simulation results for a signal line with 10 return paths using different wire models. The wire models are extracted from different inductance extraction window sizes. First, the delay simulation results using the *RC* wire model and the *RLC* wire model with the inductance model extracted from the window size including all 10 return paths are shown as reference. Then, these results are compared with the delay simulation results using the inductance models extracted from smaller extraction window sizes, the *2-Return Model* and the *4-Return Model*. The *2-Return Model* can give fairly accurate delay estimation especially for short rise times. As predicted from the  $S$ -parameter simulation results, delay estimations do not change



(a)



(b)

Figure 2.20:  $S$ -parameter extraction results with different number of return paths as in Figure 2.12.  $w = 0.5 \mu\text{m}$ ,  $d = 2 \mu\text{m}$ , and  $H = 0.8 \mu\text{m}$ . (a)  $S_{11}$ . (b)  $S_{12}$ .

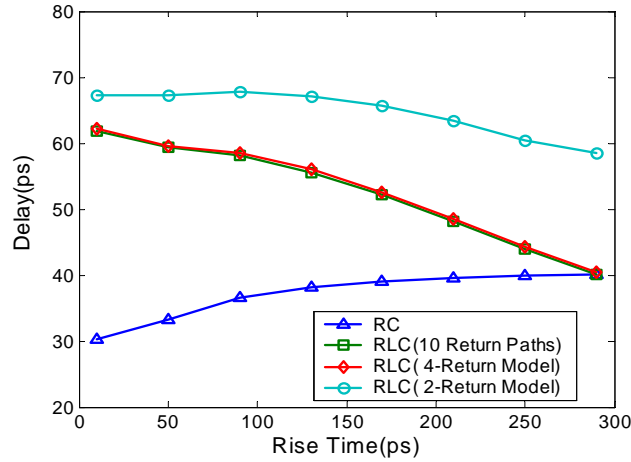


Figure 2.21: Delay simulation results of an unloaded signal line. Simulation line length is 1 mm.

much by including more return paths than the *4-Return Model*.

Current post-layout parasitic extraction tools are designed to extract  $R$  and  $C$  which have a short coupling range. Since the *4-Return Model* adds significant overhead on the extraction engine, inductance screening should be performed based on the *2-Return Model*. For more accurate extraction, an option should be provided to enlarge the extraction window to include 4 returns.

### 2.5.3 Return Current through Capacitors

In Section 2.4, it is described that FASTHENRY is based on the *magnetoquasistatic* assumption under which displacement currents through the capacitors that is shown in Figure 2.4 are neglected. However, researchers argue that as frequency increases, displacement current through the coupling capacitors will also act as the return current path [9, 10, 36]. In order to consider displacement current, full-wave field solvers should be used. In this section, we examine the accuracy of the *magnetoquasistatic*

assumption in on-chip inductance extraction.

By comparing the full-wave simulation (HFSS) and FASTHENRY simulation results, the return current through the capacitors is studied. The signal line shown in Figure 2.22(a) has coupling capacitors only in-between the parallel lines. The FASTHENRY and HFSS simulation results shown in Figure 2.23 have a negligible difference. The line structure shown in Figure 2.22(b) has very wide orthogonal lines placed on the upper and lower layer to add significant (orthogonal) capacitance. In this case, adding orthogonal lines does not change the FASTHENRY results because inductive return current flows only through the parallel lines. HFSS confirms that a portion of the return current flows though the capacitors, and the inductance is reduced especially at high frequencies. Even with this unrealistically heavy capacitive loading, the inductance difference between FASTHENRY and HFSS is less than 20% at 40 GHz. In the later part of this thesis, we will show how this change in inductance actually affects the  $RLC$  delay estimation.

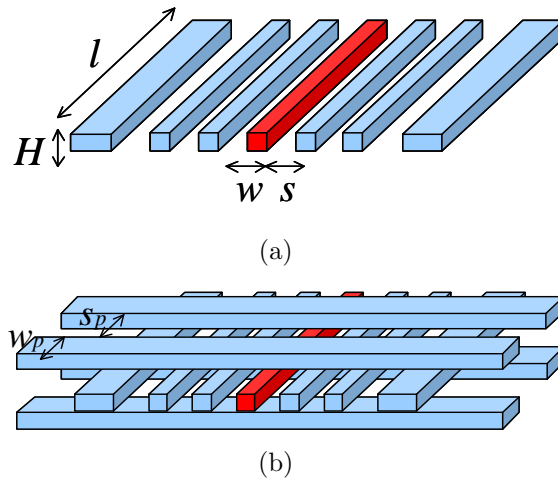


Figure 2.22: Signal line with coupling capacitors. (a) Parallel coupling  $C$  only. (b) Parallel and orthogonal coupling  $C$ .

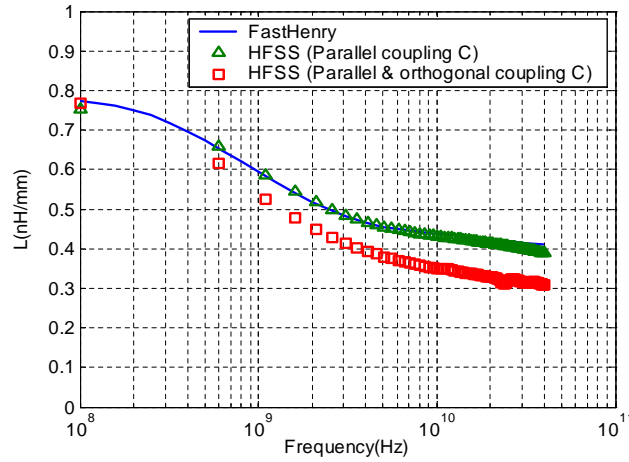


Figure 2.23: Effect of return current through capacitors.

## 2.6 Summary

The first part of this chapter provides an overview of interconnect and inductance modeling, and inductance extraction. In the second part, we examine the accuracy of the generally accepted assumptions in inductance modeling and extraction. In particular, current return path models are studied for loop inductance extraction.

An inductance model based on the closest power and ground lines, i.e. the *2-Return Model*, becomes inaccurate when line spacings are comparable to line widths or thicknesses. For accurate delay estimation, it is shown that the *4-Return Model* is sufficient. In the next chapter, we will develop an inductance screening algorithm based on inductance estimation with the *2-Return Model*. For the selected nets, more accurate inductance extraction with the *4-Return Model* can be performed.

We examine the accuracy of the *magnetoquasistatic* assumption that is used in FASTHENRY. Full-wave simulation results show that the *magnetoquasistatic* assumption is usually quite acceptable up to tens of GHz range. Since on-chip interconnects

are modeled with distributed  $RC$  or  $RLC$  segments, the capacitive return current can be considered in the distributed capacitors of the line if necessary.

## Chapter 3

# Inductance Screening Tool

The previous chapter showed the growing importance of inductance in the modeling of on-chip interconnects. Although the resistance and capacitance always need to be included in the wire model to estimate delay, the inductance effect on delay is detectable only under certain conditions [21, 22, 37]. Inductance effects occur predominantly on global interconnects which are typically wide lines located on thick upper metal layers to reduce resistance. The total number of wires in today's designs can easily exceed millions. However, the number of global interconnects is much less than that of local interconnects [38]. Even among the global interconnects, only a small number of them show inductance effects. Current static timing analysis tools cannot handle inductance, and circuit simulation including inductance is very time consuming. As a result, it would be a significant waste of resources to extract inductance for all the nets and include them in the simulations, when only a few of them actually affect the signal integrity.

In this chapter, we discuss the conditions when inductance effects are significant, develop a screening algorithm and implement a tool to identify the nets that show

inductance effects.

## 3.1 Inductance Effects

Inductance opposes an instantaneous change in current [39]. As a result, when a signal switching speed is fast enough such that the inductance effect becomes noticeable, the line delay becomes larger. Inductance also causes ringing, reflections, crosstalk noise, and simultaneous switching noise. In this section, we discuss how the line inductance affects the signal integrity and when the effect is significant.

### 3.1.1 Inductance Effects on Signal Integrity

Figure 3.1 shows a simulation setup of a wire driven by an inverter. Waveforms at the wire input and output using  $RC$  and  $RLC$  wire models are compared to show how the inductance changes the signal waveform. The inverter is designed in  $0.25\mu\text{m}$  technology with transistor sizes of  $w_p/w_n = 300/100$  and an input signal rise time of 10 ps.

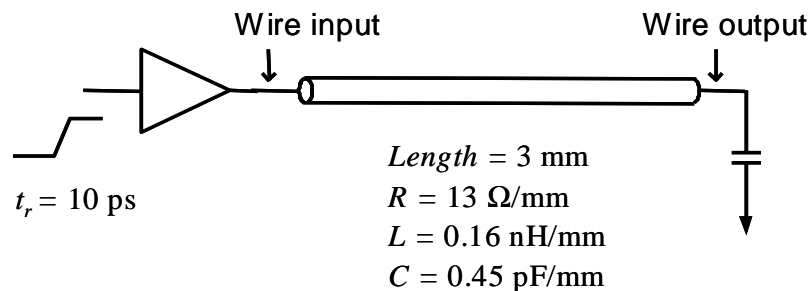
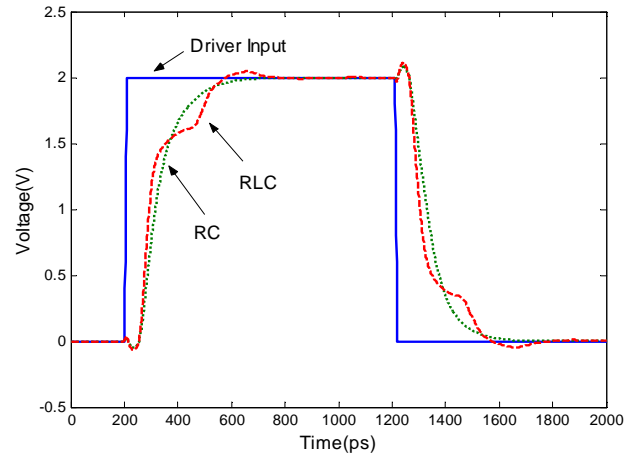
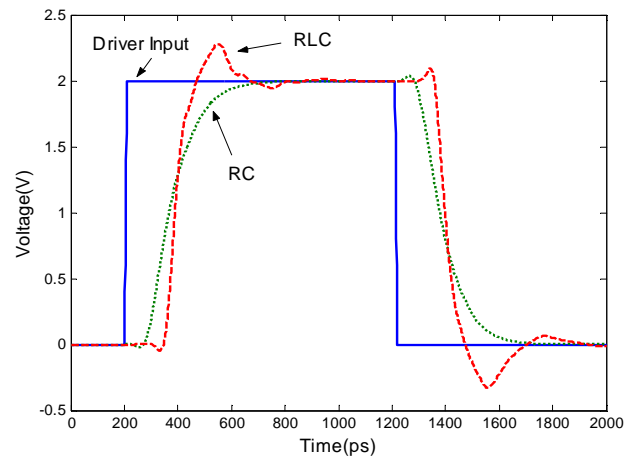


Figure 3.1: A simulation setup to compare waveforms using different wire models.



(a)



(b)

Figure 3.2: Waveform comparison using  $RC$  and  $RLC$  model. (a) Wire input. (b) Wire output.

Figure 3.2(a) shows the simulated waveforms at the wire input. When a  $RLC$  wire model is used, signal reflection occurs at the input due to the impedance mismatch between the driver and wire. Figure 3.2(b) shows the simulated waveforms at the wire output. The 50% delay from the wire input to output predicted from the  $RC$  wire model is 51.2 ps and the delay predicted from the  $RLC$  model is 96.1 ps. The inductance increases the signal delay. Comparison of the output waveforms shows that inductance also causes ringing and overshoot.

Crosstalk noise is the signal interference induced from other signal lines. On-chip crosstalk is primarily caused by the capacitive coupling between adjacent lines [24]. The main effect of capacitive crosstalk is an increase or a decrease in delay due to the change in the effective capacitance, when two neighboring lines switch in the opposite or same direction, respectively. As the frequency of the signal increases, the mutual inductance between two signal wires can create inductive coupling crosstalk noise in addition to the capacitive crosstalk [40, 41]. Figure 3.3 shows how the noise waveform changes when inductive crosstalk is present. The capacitive crosstalk is important

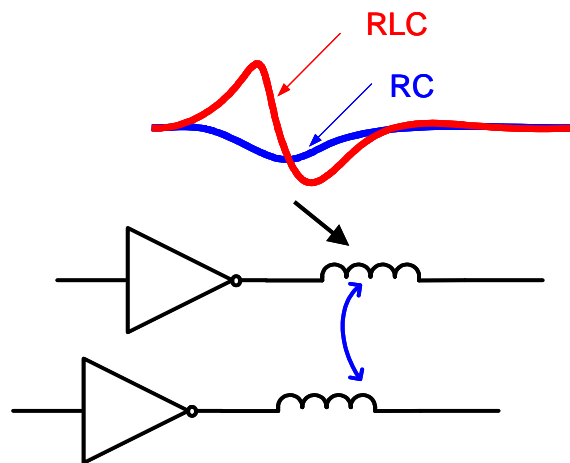


Figure 3.3: Inductive crosstalk.

only among adjacent signal lines. However, the inductive crosstalk noise is not limited to the adjacent lines due to the larger inductive coupling range.

The power supply and ground are distributed over a network composed of inductive and resistive components. The current causes IR drops across resistors and  $Ldi/dt$  across inductors. The voltage drop across the inductor is known as the simultaneous switching noise (SSN) which is shown in Figure 3.4. Until now, the SSN has been predominantly caused by the package inductance and the IR drop has been caused by on-chip power grid resistance [24]. So the on-chip power distribution networks were modeled with only resistance and capacitance. As the circuit switching speed becomes even faster, the inductive voltage drop at the on-chip power grid is starting to be important [42] and there are approaches to model the power grid as  $RLC$  transmission lines [43].

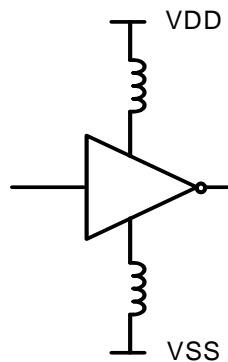


Figure 3.4: Simultaneous switching noise ( $Ldi/dt$ ) on power lines.

The inductance screening algorithm developed in this work considers inductance effects on signal delay. We will discuss how this approach can be extended to consider mutual inductance crosstalk and SSN in later chapters.

### 3.1.2 When are Inductance Effects Important?

Deustch [21] characterized on-chip interconnects by dividing them into three categories, which are short, medium and long, and developed the criteria to determine when inductance influences signal delay and crosstalk. Based on the circuit simulation results and transmission line theory, it is shown that the inductance effects depend on the driver strength, the ratio between total wire capacitance and loading capacitance, and the signal attenuation. Ismail [22] defined the rules to characterize the importance of on-chip inductance based on the signal rise time and the line damping ratio. In this work, a region where inductance effects are significant is specified for a range of line length versus input rise time. This region is expressed as Equation 3.1 and is shown in Figure 3.5.

$$\frac{t_r}{2\sqrt{LC}} < l < \frac{2}{R}\sqrt{\frac{L}{C}} \quad (3.1)$$

This figure shows that regardless of the rise time, if the wire length is longer than a certain length, the lines can be modeled with  $RC$  only because of high signal damping. As the rise time becomes smaller, more wires require inductance modeling.

We can summarize that the inductance effects are prominent when the following two conditions are satisfied:

$$R < 2\pi fL \quad (3.2)$$

$$\zeta = \frac{Rl}{2Z_0} = \frac{Rl}{2}\sqrt{\frac{C}{L}} = \frac{RCdelay}{LCdelay} \leq 1. \quad (3.3)$$

The first condition is high frequency, so that the inductive part of the line impedance becomes comparable to the resistive part. A good measure of this frequency,  $f$ , for a ramp input is known to be  $0.34/t_r$ , where  $t_r$  is the input signal rise time [27]. The second condition is low damping, or low signal attenuation [21]. The damping ratio

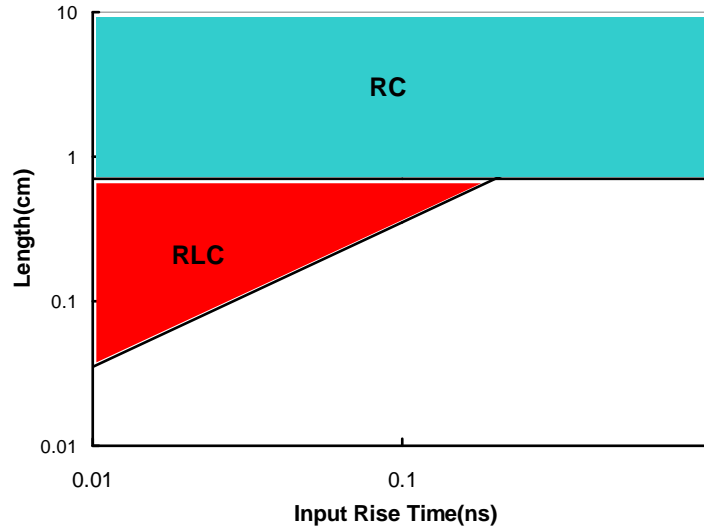


Figure 3.5: Length range of interconnect where  $RLC$  modeling is necessary.  $R = 400 \Omega$ ,  $L = 20 \text{ nH}$  and  $C = 1 \text{ pF}$ .

can also be interpreted as the ratio of  $RC$  delay over  $LC$  delay [44]. Since the  $RC$  delay has a square dependence on line length, while the  $LC$  delay has a linear dependence, the  $RC$  delay limits signal propagation for very long lines. As a result, long lines can be modeled with  $R$  and  $C$  only.

These conditions imply that the significance of inductance effects depends not only on the inductance value itself, but also on the resistance and capacitance of the line and the signal frequency. The screening conditions have a first order dependence on the values of resistances and capacitances, but has a square root dependence on the value of inductance. Hence, even with a low fidelity estimation of self inductance, inductance screening can be performed with no significant error.

## 3.2 Inductance Screening Tool

In this thesis, we develop a stand-alone screening tool that is based on standard file formats, so it can be incorporated into any design flow from various CAD vendors. Figure 3.6 shows how a screening tool can be positioned between the parasitic  $RC$  extraction step and the timing analysis step in the design flow. To perform the screening, the existing post-layout parasitic extraction tool is enhanced to include self inductance estimation.

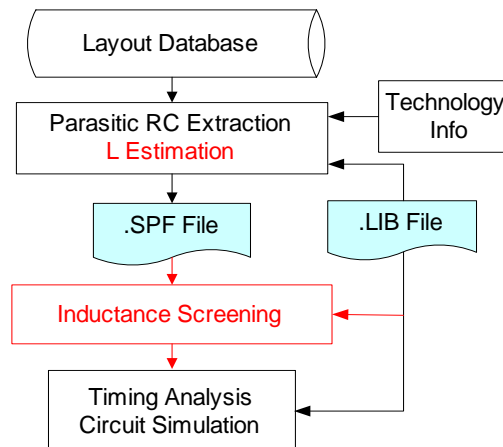


Figure 3.6: Parasitic extraction and timing verification flow. The inductance screening tool is implemented based on the standard file formats.

The .SPF file is the standard parasitic extraction output file format originally developed from Cadence and is a typical input to circuit simulators and timing analysis tools. The .LIB file is the timing technology library file generated by pre-characterizing the components of the ASIC library. This file is a standard input to circuit synthesis, gate level parasitic extraction, and timing analysis tools. Since the significance of inductance effects is a strong function of signal rise time, the rise time

information is provided from the .LIB file.

### 3.2.1 Star-RCXT and Self Inductance Estimation for Screening

In this work, the .SPF files that are used for screening are generated using Star-RCXT, a parasitic extraction tool from Synopsys [5]. Self inductance estimation based on the closest power and ground lines, the *2-Return Model*, is implemented in Star-RCXT. The extraction engine has a limit on the maximum distance it can search around its neighbor. Currently, the limit in Star-RCXT engine is set to  $10\ \mu\text{m}$ . Figure 3.7(a) shows the case when the search engine can find the power or ground line that can act as a current return path within the maximum search distance. When there is no power or ground line within the search distance, the substrate is treated as the current return path as in Figure 3.7(b).

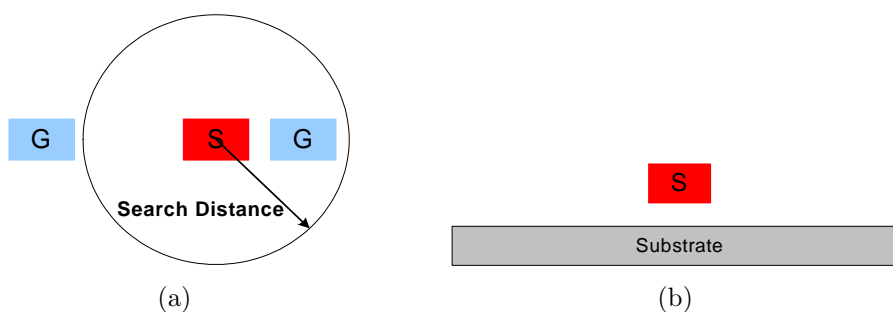
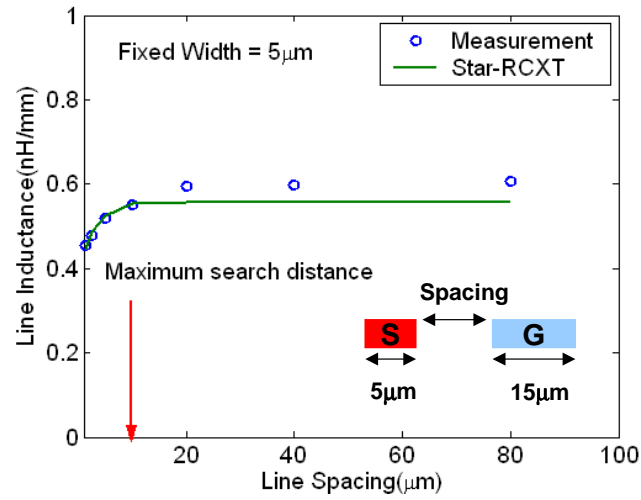
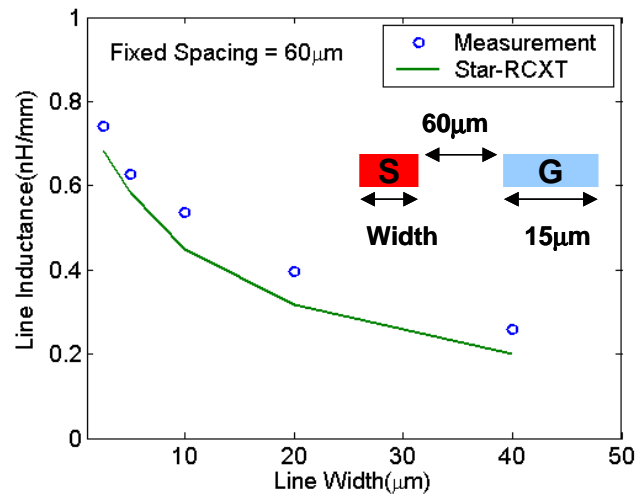


Figure 3.7: Maximum search distance. (a) Power and ground exists within search distance. (b) Power and ground does not exist within search distance.

Figure 3.8 compares the inductance values predicted from Star-RCXT and the measurement results of the test chip designed by Kleveland [44]. The test chip has a number of signal and ground line pairs on metal with different widths and spacings. Figure 3.8(a) shows how the inductance varies while the distance to the ground line



(a)



(b)

Figure 3.8: Inductance extraction and measurement comparison. (a) Spacing to the ground is varied. Fixed signal width =  $5.3\mu\text{m}$ . (b) Signal width is varied. Fixed spacing to ground =  $60\mu\text{m}$ .

varies with a fixed signal width. The measurement and Star-RCXT prediction results match well up to  $10\ \mu\text{m}$ , but the match becomes worse beyond  $10\ \mu\text{m}$  due to the search distance limitation. Figure 3.8(b) shows the case when the signal line width is varied while the spacing to the ground line is fixed. Since the fixed spacing of  $60\ \mu\text{m}$ , is larger than the search distance of Star-RCXT, the substrate is the current return path resulting in a lower accuracy. Nevertheless, the inductance dependence on signal width is correctly predicted.

### 3.2.2 Two-step Inductance Screening Algorithm

The proposed inductance screening algorithm performs the net-by-net screening in two steps as shown in Figure 3.9.

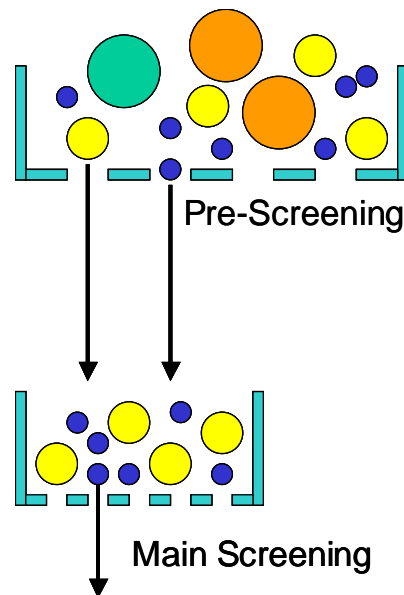


Figure 3.9: Two-step inductance screening.

The pre-screening step selects the nets that require detailed  $RC$  and  $RLC$  delay

comparison using the following criteria:

$$t_r \leq 10t_{TOF} \quad (3.4)$$

$$\zeta \leq 1.3. \quad (3.5)$$

where  $t_{TOF}$  is the time-of-flight,  $t_r$  is the signal rise time and  $\zeta$  is the damping ratio. Equation 3.4 screens out short wires that can be modeled as lumped capacitors [21, 45], and Equation 3.5 screens out long wires that have high signal attenuation.

For the nets selected in the pre-screening step, the main screening step selects the nets which have a large discrepancy between  $RC$  and  $RLC$  delay. The criteria is to compare the difference of  $RC$  and  $RLC$  delay estimates to a certain percentage,  $\gamma$ , of the rise time as the following:

$$\Delta t_d \geq \gamma \cdot t_r \quad (3.6)$$

$$\Delta t_d = t_d(RLC) - t_d(RC)$$

where  $t_r$  is the signal rise time, and  $t_d(RC)$  and  $t_d(RLC)$  are the 50%  $RC$  and  $RLC$  delays determined from the delay models that will be discussed in Chapter 4.  $\gamma$  determines the selectivity of the inductance screening, usually specified between 0.1 and 0.3. Since smaller rise time means higher clock frequency, and a faster clock requires a tighter error range in the delay estimation, the right hand side of Equation 3.6, which is the acceptable error margin in the delay difference, was chosen to be proportional to  $t_r$ .

### 3.2.3 Screening Tool Implementation

An overview of the screening tool is shown in Figure 3.10. The screening tool was implemented in C language.

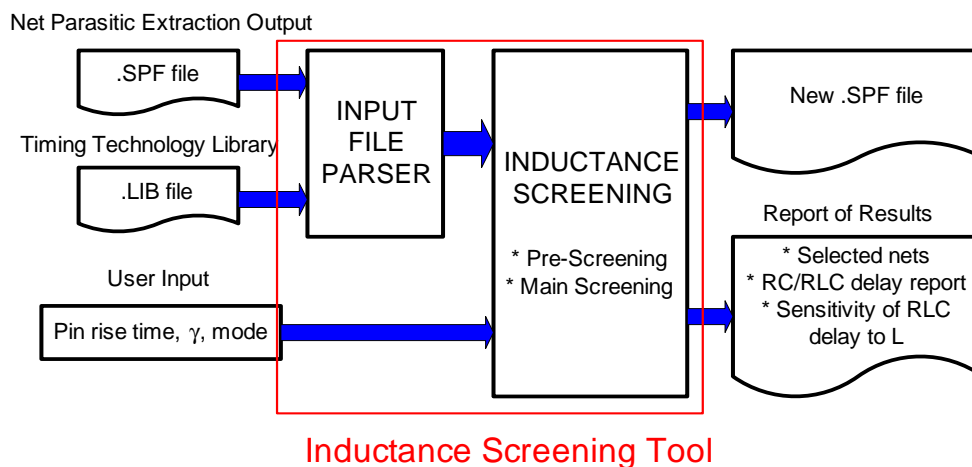


Figure 3.10: Inductance screening tool overview.

The input file parser reads in the net parasitic information from the .SPF file and the cell pin rise time information from the .LIB file. User input *mode* (fast, medium, or slow) specifies which rise time should be used from the .LIB file for inductance screening. The *pin rise time* is used as the signal rise time for I/O pins and as a default rise time if the library does not exist.

The outputs of the screening tool are a new .SPF file with unnecessary inductors removed and auxiliary output files that report the list of the selected nets. In Chapter 2, the accuracies of the *2-Return Model* and the *4-Return Model* were examined. It was shown that for accurate delay estimation, it is not necessary to include more lines than the *4-Return Model*. Since inductance estimation from the *2-Return Model* presented in Section 3.2.1 may have limitations in accuracy, the sensitivity of *RLC* delay

to inductance is reported for the selected nets to decide whether further refinement based on the *4-Return Model* is necessary.

Figure 3.11 shows an example of a net connecting different cells.

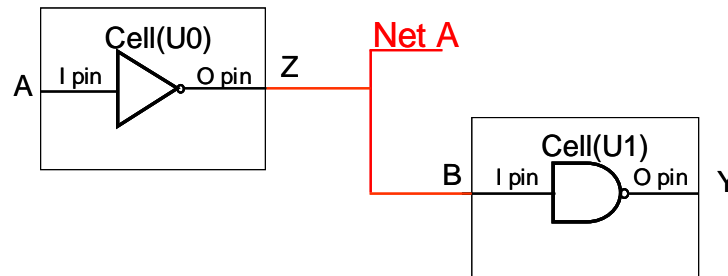


Figure 3.11: Example of an interconnect connecting two cells.

An .SPF file example representing NET A of Figure 3.11 is shown in Figure 3.12(a). At the beginning of each net definition, the names of the instance pins belonging to that net are defined. At the end of the .SPF file, there is an instance section that specifies the types of cells that are connected to each instance pin. The .LIB file is provided by the ASIC designers and has the cell output pin rise time information in a tabular format as a function of cell input rise time and capacitive loading. Figure 3.13 shows how a standard cell is characterized to derive this timing information. Figure 3.12(b) shows how the timing information of Cell(U0) is represented in the .LIB file.

The input file parser parses the net section of the .SPF file net-by-net, forming a graph structure as shown in Figure 3.14. The input parser reads in the names of the instance pins and subnodes which correspond to the vertexes of the graph structure. Each vertex has a capacitance value associated with it and each edge has a resistance and an inductance associated with it. The vertex and the edge information is saved using static hashing and the graph is formed by mapping the incident edge in the

```

*| NET A
*| I PinNameX U0 Z O cap_value loc_x loc_y
*| I PinNameY U1 B I cap_value loc_x loc_y
...
C1 PinNameX 0 cap_value
C2 PinNameY 0 cap_value
C3 sub0 0 cap_value
R1 ...
R2 ...
L1
*Instance Section
XU0 PinNameX PinNameZ VDD GND inv
XU1 PinNameY PinNameQ VDD PinNameP GND nand2b

```

(a)

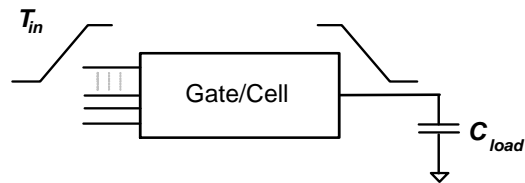
```

cell(inv)
pin(A)
direction:input
capacitance:cap_value
pin(Z)
direction:output
rise_transition, fall_transition, rise_delay, fall_delay
f(input_net_transition, total_output_net_capacitance)

```

(b)

Figure 3.12: Example of .SPF file and .LIB file describing Figure 3.11. (a) Representation of Net A in .SPF file. (b) Representation of a Cell(U0) in .LIB file.



$$\text{Gate Delay} = f(T_{in}, C_{load})$$

$$\text{Output Transition Time} = f(T_{in}, C_{load})$$

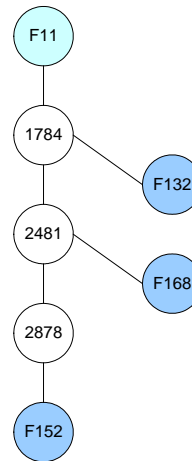
Figure 3.13: Characterization of a cell to form a library file.

```

*|NET 2 0.0386155PF
*I| (F11 0/47 Z O 0 -257 14)
*I| (F168 3/48/72 C I 1.89e-14 -136 18)
*I| (F132 3/33/50 C I 1.93e-14 -238 24.5)
*I| (F152 3/44/68 B I 1.92e-14 -81.5 19.5)
*S (2878 -82 10)
*S (1784 -238 10)
*S (2481 -136 10)
Cg36 F11 0 1.04138e-14
Cg37 2878 0 3.69095e-15
Cg38 1784 0 9.96274e-15
Cg39 2481 0 1.34501e-14
Cg40 F168 0 3.19685e-16
Cg41 F132 0 5.16911e-16
Cg42 F152 0 2.61313e-16
R29 F11 500000029 0.902133
L20 500000029 1784 1.90133e-11
R30 2878 F152 0.502403
R31 2878 500000031 2.25113
L22 500000031 2481 3.51122e-11
R32 1784 500000032 5.46144
L24 500000032 2481 3.3943e-11
R33 1784 F132 0.654319
R34 2481 F168 0.458007

```

(a)



(b)

Figure 3.14: Net representation in an .SPF file. (a) Example of a net in an .SPF file. (b) Example net represented in a graph structure.

adjacency-list. Starting from the net input vertex, the breadth-first-search spanning tree is defined by marking the parent of each vertex [46]. The .LIB file information is stored in a cell type table containing the min/max and rise/fall time for each pin type.

### 3.3 Summary

In this chapter, we review the conditions under which the inductance effects become important. The two-step screening algorithm is developed based on the inductance effect on delay. A stand-alone inductance screening tool is implemented in C language. In the next chapter, we will show the  $RC$  and  $RLC$  delay models that are used to perform screening. The test chip screening results will be presented in Chapter 5.

# Chapter 4

## Parameterized RC and RLC Delay Models

In the previous chapter, the two-step inductance screening algorithm was proposed. The pre-screening step screens out short wires that can be modeled as lumped capacitors and long wires that have high signal attenuation. The main screening is performed by computing the  $RC$  and  $RLC$  delay and comparing the difference to a certain percentage of the signal rise time.

The total number of nets in a modern IC design can easily exceed millions. The proposed screening algorithm is performed on all the nets. Therefore, not only the accuracy but also the efficiency of the delay models is critical for this application. Efficient delay models are useful for timing-driven physical design, synthesis and optimization tools as well [47].

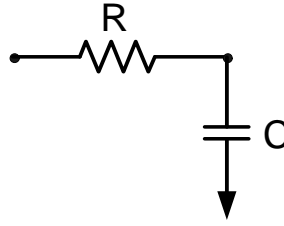
In this chapter, we review the Elmore delay model and examine the major sources of inaccuracies. The Elmore delay model is the most popular and efficient delay model. However, there are two major limitations. First, it does not take into account the

finite input signal rise time and line inductance [48, 19, 14]. Second, it significantly overestimates the delays at near-end nodes (i.e. near the driver or source) [47, 49]. We present a new approach based on nondimensionalization to derive *RC* and *RLC* delay formulae that account for the input rise time. Through nondimensionalization, a minimal set of independent parameters can be derived to characterize the delay. In Chapter 2, it was shown that using the *2-Return Model* to estimate inductance for screening has some limitations in the accuracy. Therefore, it is desirable to establish a criteria to decide whether more accurate inductance extraction is necessary for the nets that are selected from the inductance screening tool. Based on the *RLC* delay formula developed in this chapter, we derive the sensitivity of *RLC* delay to inductance. We develop a new correction factor to improve the delay estimation at the near-end nodes. This correction factor is very simple to calculate and can be implemented with no additional overhead while calculating the Elmore delay.

## 4.1 Elmore Delay Model and Its Limitations

If  $h(t)$  is the transfer function or the system impulse response, the 50% delay of the step response is the time,  $\tau$ , at which  $\int_0^\tau h(t)dt = 0.5$ . This is equivalent to the *median* of the impulse response. Elmore's approach is to approximate the *median* of the impulse response to the *mean*. The mean of the impulse response is equivalent to the negative of the first moment, which is  $\int_0^\infty th(t)dt$  [13]. For a single *RC* segment shown in Figure 4.1, Elmore proposed the time constant  $\tau$ , the 50% delay, to be *RC*, and later Wyatt proposed that the actual delay is  $0.693\tau$  [50].

Rubinstein [51] generalized the time constant approach to *RC* tree structures.

Figure 4.1: A single  $RC$  segment.

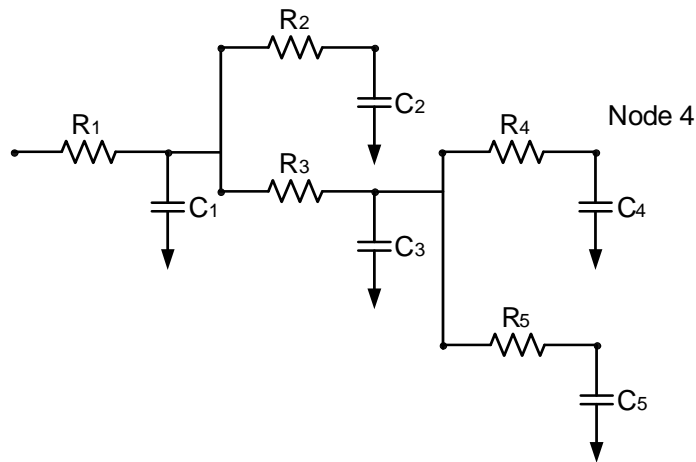
The time constant  $\tau$  for an  $RC$  tree structure is the following:

$$\tau = \sum_i R_i C_{iT}, \quad (4.1)$$

where  $R_i$  is the resistance of a section in the path, and  $C_{iT}$  is the total load capacitance of that section. For an example tree structure given in Figure 4.2, the time constant to the Node 4 can be calculated as follows:

$$\tau_{Node4} = R_1(C_1 + C_2 + C_3 + C_4 + C_5) + R_3(C_3 + C_4 + C_5) + R_4C_4 \quad (4.2)$$

Since the Elmore delay model is based only on the first moment of the impulse response, there are several limitations in its accuracy. The accuracy can be improved by determining the higher order moments of the circuits [20]. Based on these moments, the time domain waveform can be determined for arbitrary inputs [52]. However, to compute the higher order moments, additional tree traversals are required, and the delay needs to be obtained numerically. This approach involves intensive computing and is inappropriate for our screening algorithm or any physical design and optimization tools which require efficient delay evaluation for millions of nets.

Figure 4.2:  $RC$  tree example.

The original Elmore delay metric is accurate only for a step excitation. However, the typical waveform at the driving point of an interconnect is a ramp signal. Previous approaches to enhance Elmore's original concept include interpreting the impulse response of a linear circuit as a probability density function (PDF) [53, 54] and finding the higher order moments [19]. The method proposed by Kay [53] requires table construction, which becomes difficult when the input slews vary over a wide range. Kashyap [54] considered the finite rise time by convoluting the step response with the input waveform. This approach requires the mean and standard deviation for two independent PDF's, which is time consuming. Gupta [48] proved that the Elmore delay is the absolute upper bound of the actual delay and the lower bound is developed from the second moment of impulse response.

The second drawback of the Elmore delay model is the overestimation of delay at the near-end nodes [47]. This overestimation comes from the resistive shielding of the downstream capacitance. For a distributed  $RC$  line shown in Figure 4.3, the delay overestimation is worst for node 1 and the accuracy improves for nodes

farther from the signal source. The Elmore time constant at node 1 is given as  $R_1$  multiplied by the total downstream capacitance,  $C_1 + C_2 + C_3 + C_4 + C_5$ . However, the effective capacitance, which determines the actual delay, is smaller than the total capacitance and is a function of the downstream resistance. To improve the delay estimation, Alpert [49] proposed the two moment based metric (D2M) and effective capacitance based metric (ECM). However, both of these methods require additional tree traversals and increase the computation time.

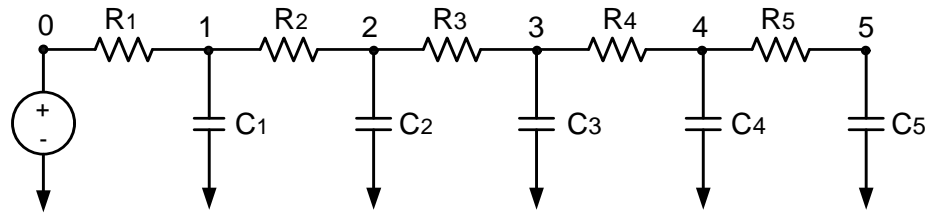


Figure 4.3: Resistive shielding.

In Chapter 2, it is shown that as clock frequency increases and the line resistance decreases with the adoption of copper technology, the line inductance becomes important. Hence, new delay models are required for  $RLC$  lines. The first attempt to derive an analytical Elmore delay for a  $RLC$  line with a step excitation was published by Kahng [15]. These models were based on the first and second moments of the line. However, there are different formulae for different damping conditions and no closed form solution exists for the moments that are used in the delay expression. Ismail [14] published simple delay models for  $RLC$  trees which are based on the second order approximation of the transfer function and preserve the recursive properties of the Elmore model. In this work, the transfer function of an  $RLC$  tree is approximated

to a second order system as the following:

$$H(s) = \frac{\omega^2}{s^2 + 2\zeta\omega s + \omega^2} \quad (4.3)$$

The transfer function is characterized by two parameters, the damping ratio  $\zeta$  and the natural frequency  $\omega$ .

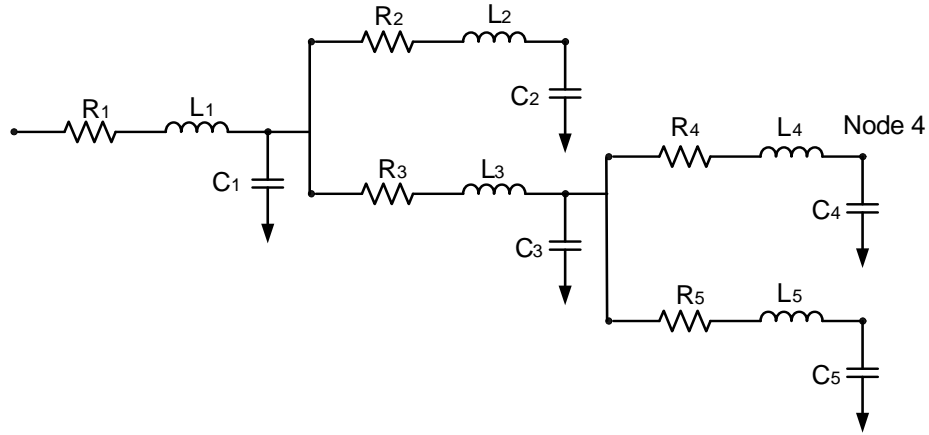
$$\zeta = \frac{1}{2} \frac{\sum_i R_i C_{iT}}{\sqrt{\sum_i L_i C_{iT}}}, \quad \omega = \frac{1}{\sqrt{\sum_i L_i C_{iT}}} \quad (4.4)$$

where  $R_i$  and  $L_i$  are the resistance and inductance of a section in the path, and  $C_{iT}$  is the total load capacitance of that section.

For an *RLC* tree in Figure 4.4,  $\zeta$  and  $\omega$  at Node 4 can be calculated from the following *RC* and *LC* summation.

$$\begin{aligned} \sum_i R_i C_{iT} &= R_1(C_1 + C_2 + C_3 + C_4 + C_5) + R_3(C_3 + C_4 + C_5) + R_4 C_4 \\ \sum_i L_i C_{iT} &= L_1(C_1 + C_2 + C_3 + C_4 + C_5) + L_3(C_3 + C_4 + C_5) + L_4 C_4 \end{aligned} \quad (4.5)$$

Although the dependence of *RLC* delay on input waveform shape is briefly mentioned in this work, no complete and accurate *RLC* delay models considering the finite input rise time have been proposed yet. Since the impact of inductance on delay is a strong function of signal rise time, we can anticipate that the dependence of *RLC* delay on input rise time is more sensitive than that of the *RC* delay.

Figure 4.4: An *RLC* tree example.

## 4.2 Delay Models Considering Ramp Input

In this section, new *RC* and *RLC* delay models are developed based on the nondimensionalization of the system governing equations and the input. Nondimensionalization is a popular technique used in fluid dynamics and quantum mechanics to identify the minimum set of independent parameters that characterize the system response [55, 56]. Nondimensionalization makes it possible to derive parameterized delay formulae and understand how the delay changes as a function of interconnect parameters and input rise time. The parameterized delay formula also enables the derivation of the sensitivity of *RLC* delay to inductance.

### 4.2.1 New Delay Model Derivation Considering Ramp Input

An *RC* tree is approximated to a first order system characterized by the time constant,  $\tau$ , shown in Equation 4.1. The governing equation is the following:

$$\tau \frac{\partial v_{out}(t)}{\partial t} + v_{out}(t) = v_{in}(t) \quad (4.6)$$

For an *RLC* tree, the governing equation is approximated to a second order system which is characterized by  $\zeta$  and  $\omega$  as the following:

$$\frac{\partial^2 v_{out}(t)}{\partial t^2} + 2\zeta\omega \frac{\partial v_{out}(t)}{\partial t} + \omega^2 v_{out}(t) = v_{in}(t) \quad (4.7)$$

where  $\zeta$  and  $\omega$  for an *RLC* tree structure are shown in Equation 4.4 [14].

The ramp input is the following:

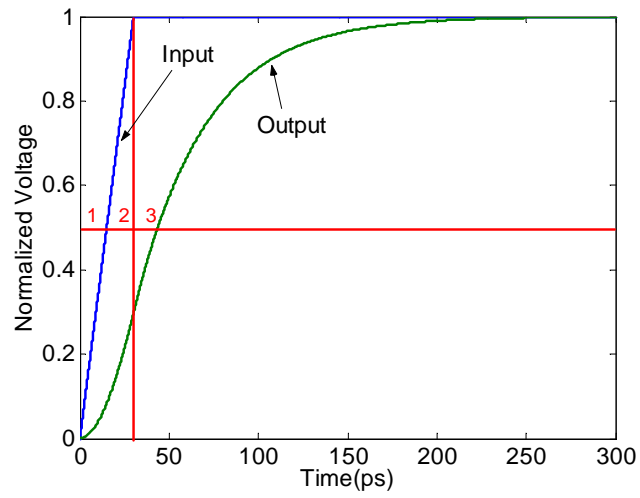
$$v_{in}(t) = \begin{cases} \frac{V_{dd}}{t_r} t & (0 \leq t \leq t_r) \\ V_{dd} & (t_r \leq t) \end{cases} \quad (4.8)$$

To derive the *RC* delay,  $t$  is nondimensionalized by dividing it with  $\tau$ . As  $\tau$  has a dimension of time,  $t/\tau$  is dimensionless. The ramp input is normalized by  $V_{dd}$ . The nondimensionalized *RC* tree governing and input equations in terms of  $\bar{t} = t/\tau$  are as follows:

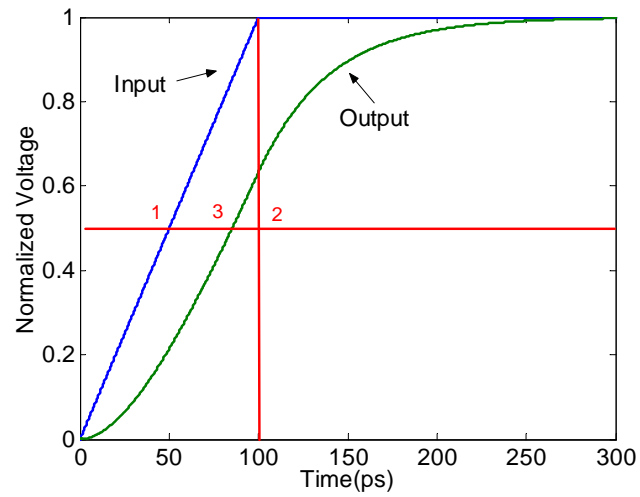
$$\frac{\partial \bar{v}_{out}(\bar{t})}{\partial \bar{t}} + \bar{v}_{out}(\bar{t}) = \bar{v}_{in}(\bar{t}) \quad (4.9)$$

$$\bar{v}_{in}(\bar{t}) = \begin{cases} \frac{1}{t_r/\tau} \bar{t} & (0 \leq \bar{t} \leq t_r/\tau) \\ 1 & (t_r/\tau \leq \bar{t}) \end{cases} \quad (4.10)$$

Equation 4.9 is independent of circuit parameters and Equation 4.10 depends only on  $t_r/\tau$ , the nondimensionalized input rise time. Hence, the output waveform with respect to nondimensionalized time is uniquely determined by one parameter,  $t_r/\tau$ . We will call the mapping from  $t_r/\tau$  to  $\bar{t}_d$ ,  $f_{RC}(t_r/\tau)$ . For fast inputs as in Figure 4.5(a), where the output waveform does not reach the 50% delay point before the ramp input reaches  $V_{dd}$  ( $\bar{v}_{out}(t_r/\tau) \leq 0.5$  or  $t_r/\tau \leq 1.6$ ), a closed form solution for the 50% delay can be found. For slow input as in Figure 4.5(b), even though the



(a)



(b)

Figure 4.5: Output waveform for  $RC$  line with different rise times. (a) Fast input. (b) Slow input.

waveform has an analytic expression with respect to  $\bar{t}$ , it cannot be solved for  $\bar{t}_d$ .  $\bar{t}_d$ 's are found numerically and a curve is formed to fit those numerical solutions. The derivation and the curve-fitting process are shown in Appendix A. Finally, the nondimensionalized  $RC$  delay can be expressed in a simple algebraic form as the following:

$$f_{RC}(t_r/\tau) = \begin{cases} \ln \left[ \frac{2}{t_r/\tau} (1 - e^{-t_r/\tau}) \right] + \frac{t_r/\tau}{2} & (t_r/\tau \leq 1.6) \\ 1 - \exp \left[ -1.14 (t_r/\tau)^{0.69} \right] & (t_r/\tau > 1.6) \end{cases} \quad (4.11)$$

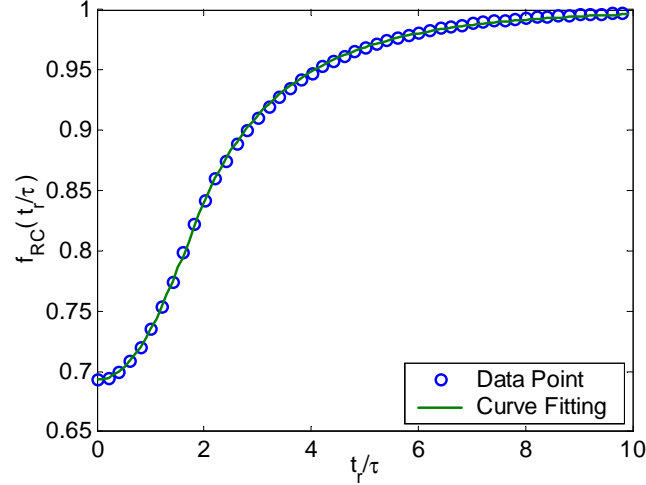
The top equation is a closed form solution and the bottom is a numerical one. The actual 50% delay can then be found from the dimensionless delay.

$$t_d = \tau f_{RC}(t_r/\tau). \quad (4.12)$$

Figure 4.6 shows that  $\tau$  corresponds to the upper bound of the  $RC$  delay, which occurs at infinite input rise time. This is consistent with the bounds reported by Gupta [17]. Our model shows that the input rise time can affect the  $RC$  delay by as much as 30%, which is less than the percentage claimed by others [19].

To derive the  $RLC$  formulas,  $t$  is nondimensionalized by multiplying it with the natural frequency  $\omega$ , which has the dimension of inverse of time. The nondimensionalized governing equation for  $RLC$  trees and the normalized input are as follows:

$$\frac{\partial^2 \bar{v}_{out}(\bar{t})}{\partial \bar{t}^2} + 2\zeta \frac{\partial \bar{v}_{out}(\bar{t})}{\partial \bar{t}} + \bar{v}_{out}(\bar{t}) = \bar{v}_{in}(\bar{t}) \quad (4.13)$$

Figure 4.6: Dimensionless  $RC$  delay.

$$\bar{v}_{in}(\bar{t}) = \begin{cases} \frac{1}{\omega t_r} \bar{t} & (0 \leq \bar{t} \leq \omega t_r) \\ 1 & (\omega t_r \leq \bar{t}) \end{cases} \quad (4.14)$$

After the nondimensionalization, the governing equation depends only on  $\zeta$ , and the ramp input is characterized by  $\omega t_r$ . So, the dimensionless delay  $\bar{t}_d$  can be expressed in terms of  $\zeta$  and  $\omega t_r$ , as  $f_{RLC}(\zeta, \omega t_r)$ . The ranges of  $\zeta$  and  $\omega t_r$  are set by the pre-screening conditions, Equations 3.4 and 3.5, which are  $0 \leq \zeta \leq 1.3$  and  $0 \leq \omega t_r \leq 10$ . These conditions correspond to the ranges where inductance is important. For  $\zeta$ 's larger than 1.3, the  $RC$  delay model is sufficient, because there is a high signal attenuation. Since  $\omega$  is equivalent to the inverse of time-of-flight,  $\omega t_r$  larger than 10 corresponds to short wires which can be treated as lumped capacitors. In the ranges of  $\zeta$  and  $\omega t_r$  when  $RLC$  delay modeling is necessary, numerical solutions show that for a given  $\omega t_r$ , the dimensionless delay,  $\omega t_d$ , can be approximated by a straight line.

$$f_{RLC}(\zeta, \omega t_r) = a_1(\omega t_r) \zeta + a_0(\omega t_r) \quad (4.15)$$

Expressions for  $a_1$  and  $a_0$  are approximated by third order polynomials with respect to  $\omega t_r$ .

$$\begin{aligned} a_1(\omega t_r) &= -0.003(\omega t_r)^3 + 0.047(\omega t_r)^2 + 0.014(\omega t_r) + 0.69 \\ a_0(\omega t_r) &= 0.003(\omega t_r)^3 - 0.048(\omega t_r)^2 + 0.051(\omega t_r) + 0.96 \end{aligned} \quad (4.16)$$

The derivation is done using the least square method, and the details of the derivation are shown in Appendix A.

The actual *RLC* delay can be found by dividing the dimensionless delay by  $\omega$ .

$$t_d = \frac{1}{\omega} f_{RLC}(\zeta, \omega t_r) \quad (4.17)$$

The dimensionless *RLC* delay is shown in Figure 4.7.

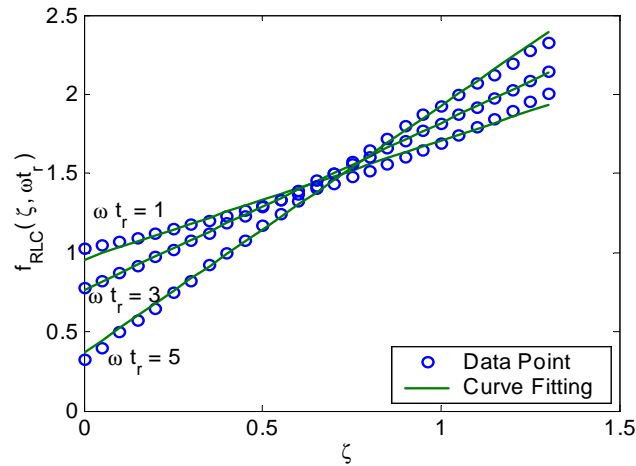


Figure 4.7: Dimensionless *RLC* delay.

From these parameterized delay models, we can predict how the delay varies as a function of line characteristics and rise time. We can see that the *RLC* delay is more sensitive to rise time than the *RC* delay. Inductance increases the delay because it opposes the instantaneous change in current. In Figure 4.7, when the lines are

inductive ( $\zeta \ll 1$ ), as rise time ( $t_r$ ) becomes shorter, the actual delay increases due to larger inductance effects. If inductance or capacitance increases,  $\omega$  decreases, so the delay increases. The equivalent Elmore delay proposed by Ismail gives the upper limit on *RLC* delay with a step input [14].

Table 4.1 shows the accuracy of the proposed delay model by comparing the delay estimation results with HSPICE. The delay estimation is performed for a sample tree structured net shown in Figure 4.8. *RC* delay is calculated by setting all the inductors in the tree structure to zero. At nodes OUT1 and OUT2, *RC* and *RLC* delays for different rise times predicted from the proposed delay metrics match well with those found from HSPICE simulations.

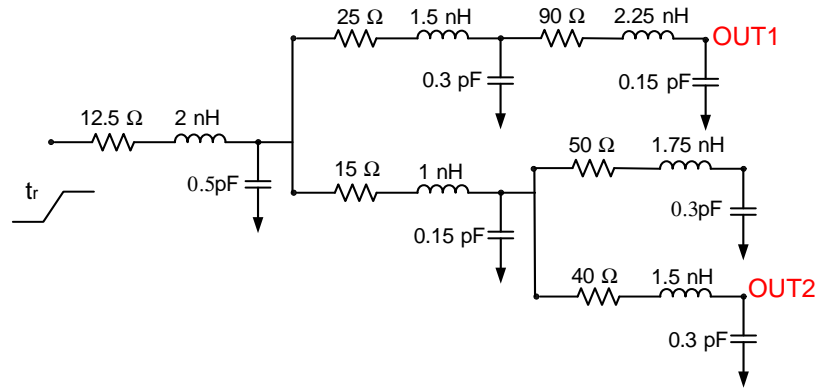


Figure 4.8: *RLC* tree example.

## 4.2.2 Sensitivity of Delay to Inductance

The sensitivity of *RLC* delay, which shows how the change in inductance affects the delay, is defined as the following:

$$\frac{dt_d}{t_d} = S \frac{dL}{L} \quad (4.18)$$

	tr (ps)	RC				RLC				
		tr/τ	Delay (ps)		Diff(%)	ζ	ωtr	Delay (ps)		Diff(%)
			Formula	HSPICE				Formula	HSPICE	
<b>OUT1</b>	<b>20</b>	<b>0.43</b>	<b>32.25</b>	<b>35.42</b>	<b>-8.96</b>	<b>0.35</b>	<b>0.30</b>	<b>80.42</b>	<b>85.88</b>	<b>-6.36</b>
	<b>100</b>	<b>2.17</b>	<b>39.43</b>	<b>41.82</b>	<b>-5.73</b>	<b>0.35</b>	<b>1.51</b>	<b>80.64</b>	<b>83.82</b>	<b>-3.79</b>
	<b>260</b>	<b>5.65</b>	<b>44.94</b>	<b>45.52</b>	<b>-1.27</b>	<b>0.35</b>	<b>3.92</b>	<b>68.92</b>	<b>68.12</b>	<b>-1.18</b>
<b>OUT2</b>	<b>20</b>	<b>0.45</b>	<b>31.22</b>	<b>33.17</b>	<b>-5.88</b>	<b>0.33</b>	<b>0.29</b>	<b>81.24</b>	<b>85.39</b>	<b>-4.86</b>
	<b>100</b>	<b>2.25</b>	<b>38.42</b>	<b>39.95</b>	<b>-3.83</b>	<b>0.33</b>	<b>1.47</b>	<b>81.41</b>	<b>84.98</b>	<b>-4.20</b>
	<b>260</b>	<b>5.84</b>	<b>43.56</b>	<b>43.97</b>	<b>-0.93</b>	<b>0.33</b>	<b>3.83</b>	<b>69.40</b>	<b>68.04</b>	<b>-2.00</b>

Table 4.1: RC and RLC delay estimation comparison with HSPICE at nodes OUT1 and OUT2.

where  $S$  is the sensitivity.

The sensitivity is calculated by taking the derivative of the dimensionless RLC delay with respect to  $L$ . Equation 4.17 can be written as the following:

$$\omega t_d = f_{RLC}(\zeta, \omega t_r) \quad (4.19)$$

Since  $f_{RLC}$  is expressed as a function of  $\zeta$  and  $\omega t_r$ , the chain rule can be applied as follows:

$$\frac{\partial}{\partial L}(\omega t_d) = \frac{\partial}{\partial L} f_{RLC} = \frac{\partial f_{RLC}}{\partial \zeta} \frac{\partial \zeta}{\partial L} + \frac{\partial f_{RLC}}{\partial (\omega t_r)} \frac{\partial (\omega t_r)}{\partial L} \quad (4.20)$$

The derivatives of  $\zeta$  and  $\omega t_r$  with respect to  $L$  are as follows:

$$\frac{\partial \zeta}{\partial L} = -\frac{1}{2L} \zeta, \quad \frac{\partial (\omega t_r)}{\partial L} = -\frac{1}{2L} (\omega t_r) \quad (4.21)$$

After rearrangements, the sensitivity  $S$  is expressed as the following:

$$S = \frac{1}{2} \left\{ -\frac{1}{f_{RLC}} \left( \zeta \frac{\partial f_{RLC}}{\partial \zeta} + (\omega t_r) \frac{\partial f_{RLC}}{\partial (\omega t_r)} \right) + 1 \right\} \quad (4.22)$$

From the final expression, we can see that  $S$  depends only on  $\zeta$  and  $\omega t_r$ .

The sensitivities as a function of the damping ratio for three different rise times are shown in Figure 4.9. In general, the delay is less sensitive to inductance than to resistance or capacitance.

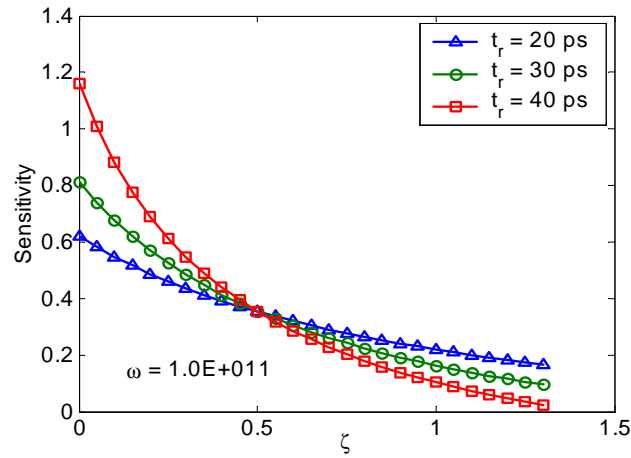


Figure 4.9: Sensitivity of  $RLC$  delay to inductance.

Figure 4.10 shows the contour plot of sensitivity. For small  $\zeta$ 's, where inductance effects are important, sensitivity increases for larger  $\omega t_r$ . For small  $\zeta$ 's and large  $\omega t_r$ 's, the sensitivity is very large, but this is due to the very small delay itself.

As described in the previous chapters, inductance screening is performed based on the inductance estimated with the *2-Return Model*. After the screening, for the selected nets with significant inductance effects, this sensitivity analysis can be used to determine whether more accurate inductance extraction using the *4-Return Model* is necessary.

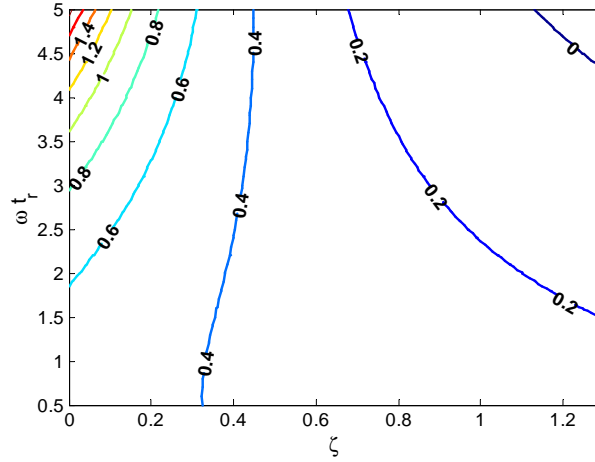


Figure 4.10: Contour plot of the sensitivity of *RLC* delay to inductance.

### 4.3 Effective Distance Correction Factor

Table 4.2 shows a comparison of the delay at node OUT0 of Figure 4.11 for different signal rise times. There is a significant overestimation in the delay especially when the rise times become fast. This overestimation comes from the resistive shielding of the downstream capacitance, because OUT0 is relatively close to the signal input. In this section, we develop a model to predict this overestimation and correct the delay estimation at the near-end nodes.

	tr (ps)	RC				RLC				
		tr/t	Delay (ps)		Diff(%)	ζ	ωtr	Delay (ps)		Diff(%)
			Formula	HSPICE				Formula	HSPICE	
<b>OUT0</b>	<b>20</b>	<b>0.94</b>	<b>15.51</b>	<b>9.82</b>	<b>57.94</b>	<b>0.18</b>	<b>0.34</b>	<b>64.01</b>	<b>43.48</b>	<b>47.22</b>
	<b>100</b>	<b>4.71</b>	<b>20.48</b>	<b>17.79</b>	<b>15.12</b>	<b>0.18</b>	<b>1.70</b>	<b>62.41</b>	<b>50.54</b>	<b>23.49</b>
	<b>260</b>	<b>12.2</b>	<b>21.25</b>	<b>20.86</b>	<b>1.87</b>	<b>0.18</b>	<b>4.46</b>	<b>43.50</b>	<b>40.97</b>	<b>6.18</b>

Table 4.2: *RC* and *RLC* delay estimation comparison with HSPICE at node OUT0.

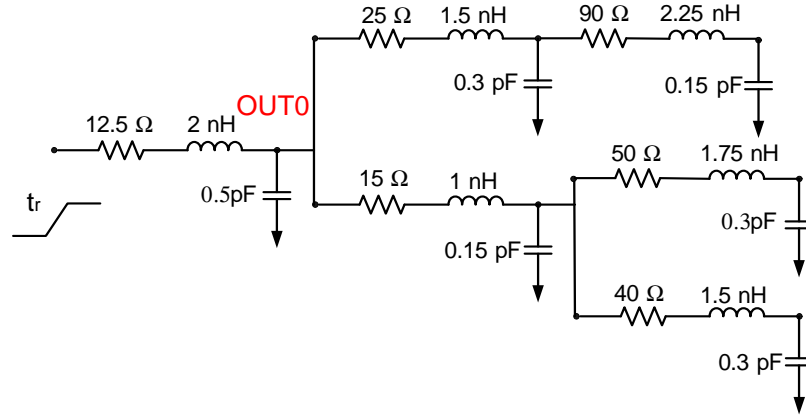


Figure 4.11: *RLC* tree example.

### 4.3.1 Signal Propagation in a Distributed RC Transmission Line and Elmore Approximation

The actual signal propagation in a distributed *RC* transmission line is governed by the following diffusion equation:

$$\frac{\partial^2 V}{\partial x^2} = \left(\frac{R}{l}\right) \left(\frac{C}{l}\right) \frac{\partial V}{\partial t} \quad (4.23)$$

where  $l$  is the length of the line, and  $R$  and  $C$  are the total line resistance and capacitance, respectively. The boundary conditions are as follows:

$$x = 0: V(0, t) = V_{in}(t) \quad (4.24)$$

$$x = l: \frac{\partial V}{\partial x} = 0 \quad (4.25)$$

Elmore's approach approximates the partial differential equation with an ordinary differential equation by removing the  $x$  derivative in Equation 4.23 and introducing

a parameter  $\tau$ . Then, the governing equation becomes as follows:

$$\tau \frac{\partial V}{\partial t} + V = V_{in} \tag{4.26}$$

where  $\tau$  has an explicit dependence on location  $x$ , given as the following:

$$\tau = \int_0^x \left( \frac{C(l-\xi)}{l} \right) \left( \frac{R}{l} \right) d\xi = \frac{RC}{2} \left( 2 \left( \frac{x}{l} \right) - \left( \frac{x}{l} \right)^2 \right) \tag{4.27}$$

Figure 4.13 shows a signal waveform at  $x/l = 0.18$ , a node that is relatively close to the signal input, for the wire shown in Figure 4.12.

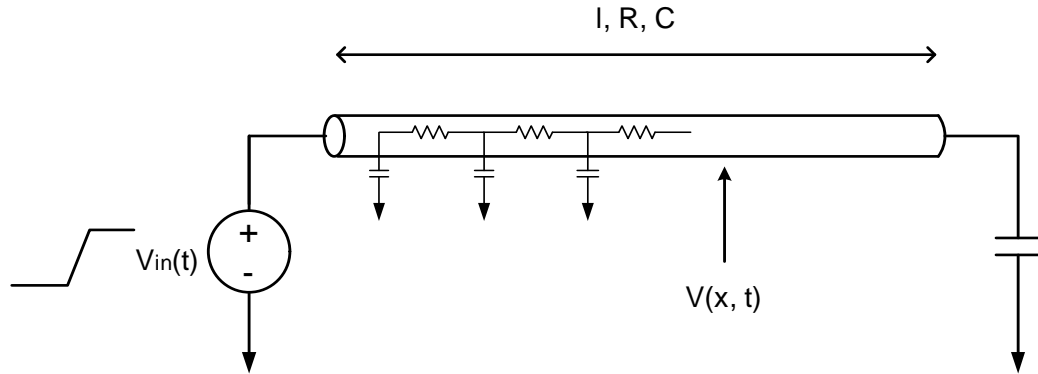


Figure 4.12: Distributed RC transmission line.

The waveform from Elmore’s approximation, Equation 4.26, reaches the 50% threshold point later than that predicted from the diffusion model, Equation 4.23. By comparing the Elmore delay with the actual delay found from the diffusion model, we can get the relative overestimation of the Elmore delay. We will call this error, the *Effective Distance Correction Factor (EDCF)*.

To develop a model for *Effective Distance Correction Factor (EDCF)*, location  $x$

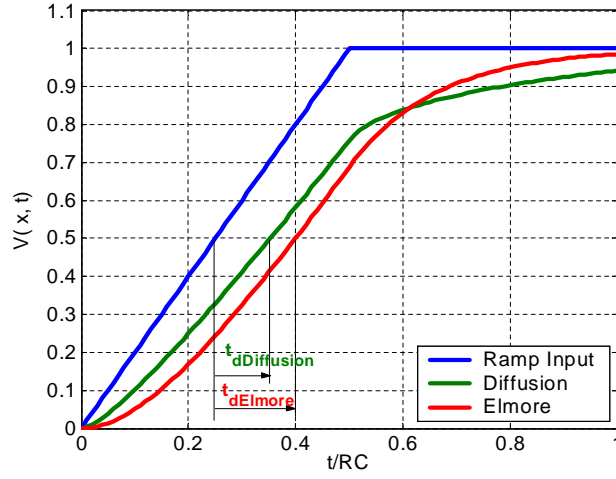


Figure 4.13: Comparison of the waveform found from the diffusion model and Elmore's approximation at a near-end node.

is nondimensionalized by dividing it by  $l$  and time  $t$  by  $RC$ .

$$\bar{x} = \frac{x}{l}, \quad \bar{t} = \frac{t}{RC} \quad (4.28)$$

The nondimensionalized governing equations for the diffusion equation and Elmore's approximation are the following:

$$\frac{\partial^2 V}{\partial \bar{x}^2} = \frac{\partial V}{\partial \bar{t}} \quad (4.29)$$

$$\frac{1}{2} (2\bar{x} - \bar{x}^2) \frac{\partial V_{out}}{\partial \bar{t}} + V_{out} = V_{in} \quad (4.30)$$

The nondimensionalized ramp input is the following:

$$V_{in}(\bar{t}) = \begin{cases} \frac{1}{t_r/RC} \bar{t} & (0 \leq \bar{t} \leq t_r/RC) \\ 1 & (t_r/RC \leq \bar{t}) \end{cases} \quad (4.31)$$

Equation 4.29 does not have a dependence on any circuit parameters. Equation 4.30 depends only on  $\bar{x}$ , which is  $x/l$ . The input is characterized by  $t_r/RC$ . So for a given relative location  $x/l$ , the waveform is uniquely determined by  $t_r/RC$ , and consequently the overestimation in the Elmore delay model is only a function of  $t_r/RC$  as well.

Equation 4.29 is solved using second order central differencing in space, and first order Euler implicit scheme in time to ensure stability as the following:

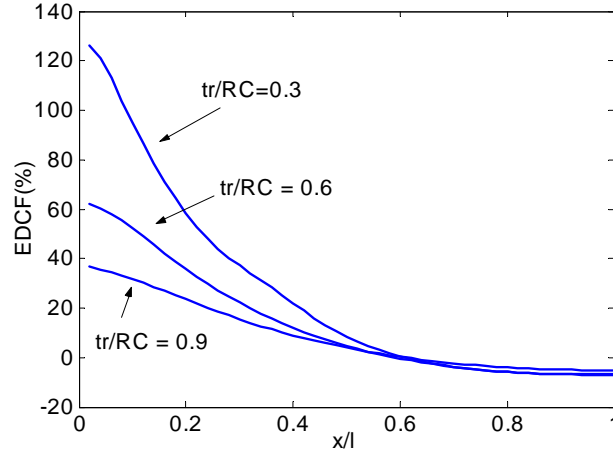
$$\frac{V_i^{n+1} - V_i^n}{\Delta \bar{t}} = \frac{V_{i+1}^{n+1} - 2V_i^{n+1} + V_{i-1}^{n+1}}{\Delta \bar{x}^2}. \quad (4.32)$$

The boundary condition given in Equation 4.24 correspond to the Dirichlet boundary condition and Equation 4.25 corresponds to the Neumann boundary condition.

By comparing the delay predicted from the diffusion model and Elmore's approximation, we can find the overestimation of the Elmore delay model, *EDCF*, at location  $x/l$  as the following:

$$EDCF\left(\frac{x}{l}\right) = \frac{t_{dElmore} - t_{dDiffusion}}{t_{dDiffusion}} \quad (4.33)$$

Figure 4.14 shows the *EDCF* for different  $t_r/RC$ 's. Regardless of the signal rise time, the error is negligible if  $x/l$  is larger than 0.6. The overestimation in Elmore's approximation worsens as the rise time decreases. This prediction is consistent with the delay simulation results shown in Table 4.2.

Figure 4.14: *Effective Distance Correction Factor (EDCF)*.

The expression for  $EDCF$  is numerically approximated with a second order polynomial of  $\bar{x}$ .

$$EDCF(\bar{x}) = \frac{t_{dElmore} - t_{dDiffusion}}{t_{dDiffusion}} \cong c_2 \bar{x}^2 + c_1 \bar{x} + c_0 \quad (4.34)$$

where  $\bar{x} = x/l$ .  $c_0$ ,  $c_1$  and  $c_2$ , are functions of  $t_r/RC$  and the process to determine these coefficients through numerical curve-fitting is shown in Appendix B. The final expression for  $EDCF$  is the following:

$$EDCF = c_2(t_r/RC)(x/l)^2 + c_1(t_r/RC)(x/l) + c_0(t_r/RC) \quad (4.35)$$

where the coefficients are as follows:

$$\begin{aligned} c_2(t_r/RC) &= 9.82e^{-3.39t_r/RC} - 0.02 \\ c_1(t_r/RC) &= -11.17e^{-3.15t_r/RC} - 0.16 \\ c_0(t_r/RC) &= 3.21e^{-2.92t_r/RC} + 0.12 \end{aligned} \quad (4.36)$$

Given the *EDCF*, the actual delay can be corrected as the following:

$$t_{dEDCF} = \frac{t_d}{1 + EDCF} \quad (4.37)$$

where  $t_d$  is the *RC* or *RLC* delay calculated from the parameterized delay equations described in the previous section, Equations 4.12 and 4.17.

### 4.3.2 EDCF in Tree Structures

Most of the nets in IC designs are tree structures. In order to apply the *EDCF* derived from a single line structure to a tree structure, we need to generalize several parameters.

From the single distributed *RC* line analysis, we know that the resistive shielding of the downstream capacitance is a function of relative distance,  $x/l$ .  $x$  is the distance from the input to the probing point, and  $l$  is the line length. For a single line structure,  $x/l$  is equivalent to the ratio of the resistance from the input to the probing point over the total line resistance. So, for a tree structure, for each fanout, we can calculate the signal path resistance from the input to the fanout. We can generalize  $x/l$  to the ratio of the signal path resistance to the maximum path resistance of a tree structure. We will call this the *Effective Distance (ED)*. For an example of a tree shown in Figure 4.15, the *ED* is calculated as follows:

$$ED = \frac{R_{path}}{Max\{R_{path}\}} = \frac{R_1 + R_2 + R_3}{R_1 + R_4 + R_5 + R_6 + R_7} \quad (4.38)$$

*RC* is the product of the total resistance and total capacitance of a single line.

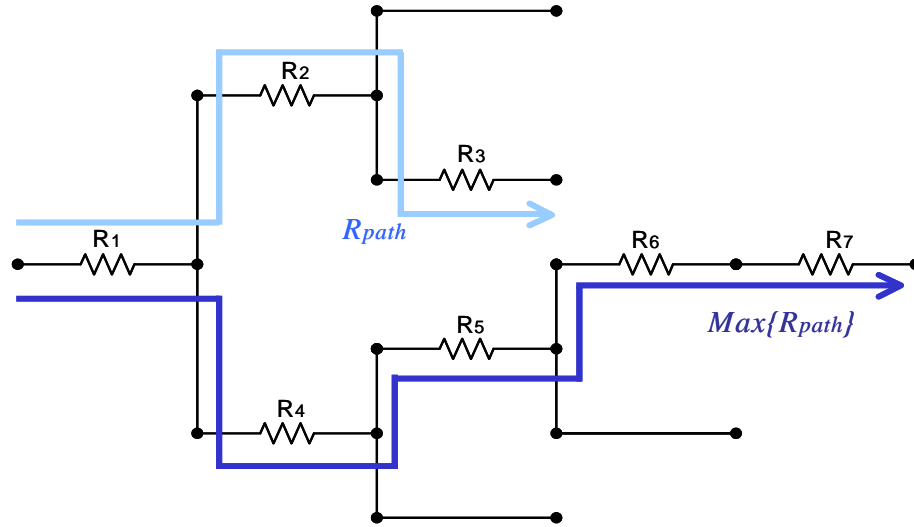
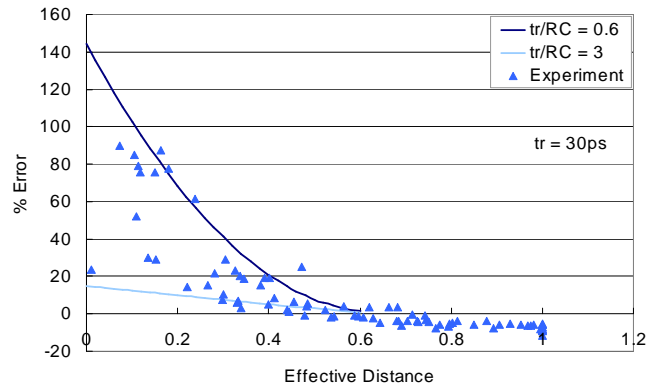


Figure 4.15: *Effective distance (ED)* for a tree structure.

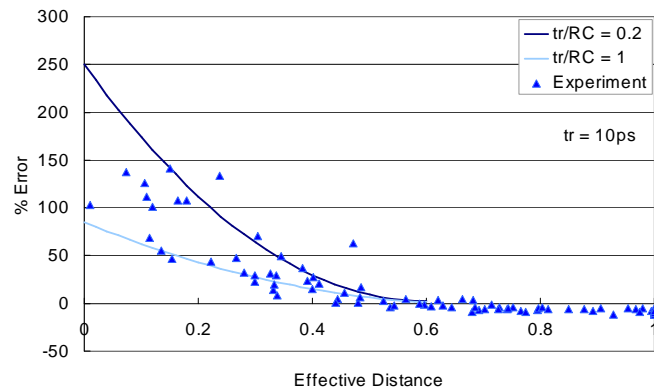
Since the Elmore time constant is  $RC/2$  for a single line structure, for a tree structure,  $RC$  can be generalized to  $2 \sum_i R_i C_{iT}$  of the fanout that has maximum path resistance. The *EDCF* for a tree structured net can be calculated with no additional tree traversals, preserving the efficiency of the Elmore delay model.

In order to see whether the *EDCF* proposed in this section works for general tree structures, we selected a number of test nets with near-end nodes from a real IC design. For every near-end node in a net, i.e.  $ED < 0.6$ , the overestimation is calculated by comparing the  $RC$  delay found from Equation 4.12 with that from the HSPICE simulation. The error points are plotted with respect to  $ED$  in Figure 4.16. Among the test nets, the maximum and minimum  $t_r/RC$ 's are determined. The solid lines show the *EDCF*'s calculated for the maximum and minimum  $t_r/RC$ 's. Figures 4.16(a) and (b) show the case for two different rise times, 30 ps and 10 ps. As predicted in Figure 4.14, *EDCF* increases as rise time decreases. This experiment verifies that the *EDCF* and the concept of  $ED$  can be applied to predict the delay

estimation errors that occur in near-end nodes of a tree structure.



(a)



(b)

Figure 4.16: Verification of the generalization of *EDCF* to tree structures using rise times of (a) 30 ps, and (b) 10 ps.

### 4.3.3 Improvement in Delay Estimation

The improvement in the accuracy of delay models using *EDCF* is verified for the test nets that were examined in the previous section. First, the delays considering the input rise time are calculated from the equations proposed in Section 4.2 and are

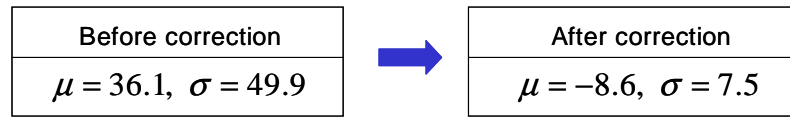
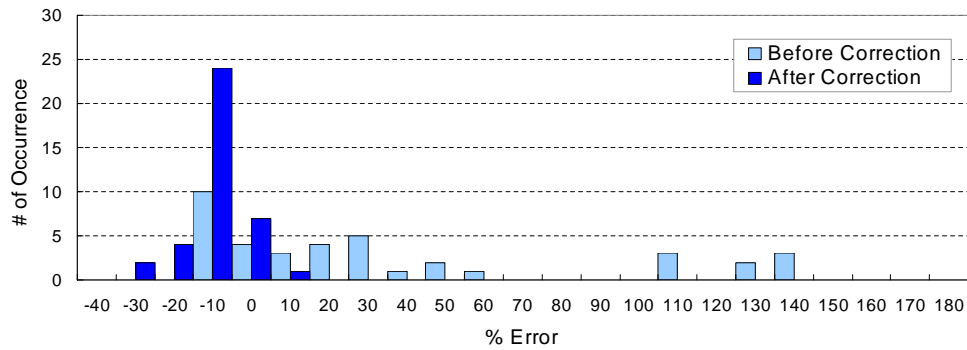
compared with the results from HSPICE simulation. The errors prior to applying the *EDCF* are shown in a histogram in Figure 4.17. Then, the *ED* is determined for every fanout in the net, and if the *ED* is smaller than 0.6, the corresponding *EDCF* is calculated. The delay is corrected by dividing it with  $1+EDCF$ , as in Equation 4.37. The errors after correction are shown in the histogram for comparison. Figure 4.17(a) shows that the *RC* delay estimation improves significantly by using *EDCF*.

The *RLC* delay metrics are derived based on  $\zeta$  and  $\omega$ , which are functions of *RC* and *LC* summation for a tree structure as shown in Equation 4.4. As a result, the *RC* and *LC* summations found for a near-end node will also have the effective capacitance overestimation due to resistive shielding. We propose to use the same correction factor for the *RLC* delay model. Figure 4.17(b) shows the *RLC* delay estimation also improves drastically by applying *EDCF*.

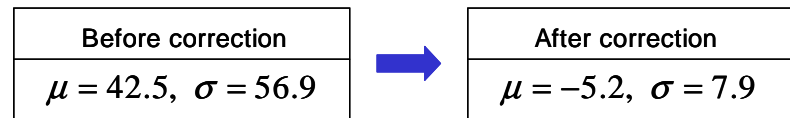
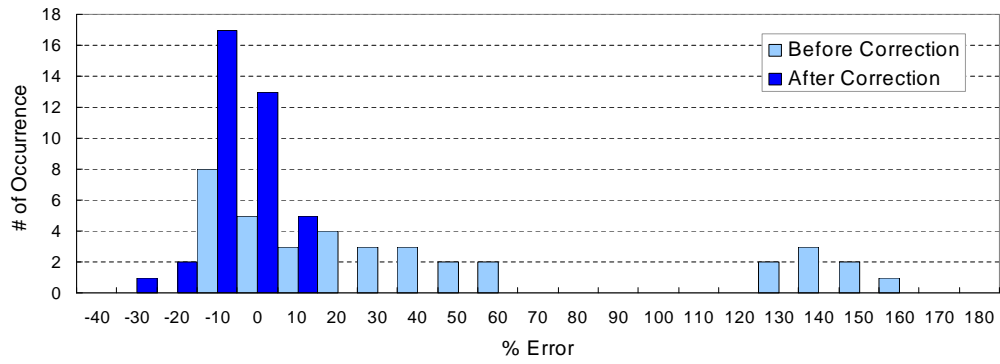
## 4.4 Summary

New *RC* and *RLC* delay models, considering the input rise time and retaining the efficiency and simplicity of the Elmore delay model, is developed to perform inductance screening. From the parameterized delay models, we can derive the sensitivity of *RLC* delay to inductance and understand how the delay changes as the line parameters and the input rise time vary.

We propose a new correction method to consider resistive shielding of downstream capacitance. The correction method works well for both *RC* and *RLC* delay models. Efficient delay models in an algebraic form are critical for timing-driven physical design, synthesis and optimization tools.



(a)



(b)

Figure 4.17: Delay improvement using *EDCF* for (a) *RC* delay, and (b) *RLC* delay.

# Chapter 5

## Experimental Results

A stand-alone inductance screening tool was developed in C language based on the algorithm described in Chapter 3. The pre-screening step selects the nets that require a detailed  $RC$  and  $RLC$  delay comparison at the main screening step. Usually, at the pre-screening step, around 5 – 10% of the total nets are selected, which significantly narrows down the number of nets that require the main screening. The main screening is performed based on the delays found from the formulae described in Chapter 4. The main screening is done based on the following criteria:

$$t_d(RLC) - t_d(RC) \geq \gamma \cdot t_r \quad (5.1)$$

The user specifies  $\gamma$ , which determines the selectivity of screening. Typical value of  $\gamma$  is between 0.1 and 0.3.

The input files for the inductance screening tool are .SPF and .LIB files. A parasitic extraction tool from Synopsys, Star-RCXT, is used to generate .SPF files [5]. In running the parasitic extraction, the extraction options need to be specified in

the *star\_cmd* file. In order to get the self inductance estimation required to perform the screening, we need to specify the extraction mode to be *RLC* and specify the names of the power/ground nets. All loops need to be removed such that all the nets are in a tree structure. This transformation is automatically done at the Star-RCXT netlisting stage based on a  $\Delta - Y$  conversion [39] by specifying an option in the *star\_cmd* file. In summary, the commands that should be included in the *star\_cmd* file to generate a proper input file for the screening tool are the following:

- EXTRACTION : RLC
- POWER\_NETS: VDD GND
- NETLIST\_REMOVE\_LOOPS : YES

The .LIB file is provided by the standard cell designers. If a .LIB file is not available, the user can specify the rise time for the screening.

In this chapter, we show the inductance screening results of three IC designs and suggest ways to reduce the inductance effect for the selected nets by increasing the input rise time or modifying the interconnect design.

## 5.1 Test Chip Screening Results

In this section, we show the inductance screening results of these test chips. The screening results are verified by performing circuit simulations on the selected nets. The net length distributions of the selected nets are examined and compared with theoretical predictions.

### 5.1.1 Stanford Inductance Test Chip

The first case is a test chip fabricated by Kleveland [44] in a 5 metal layer using  $0.25\mu\text{m}$  technology. The screening was performed for 22, 4 mm signal lines located on the top metal layer. The geometries of the tested lines are shown in Table 5.1.

(a)			(b)		
Net Name	Signal Width( $\mu\text{m}$ )	Spacing to GND( $\mu\text{m}$ )	Net Name	Signal Width( $\mu\text{m}$ )	Spacing to GND( $\mu\text{m}$ )
1	5	5	1	5	5
2	40	60	2	40	60
3	5	70	3	5	70
4	10	75	4	10	75
5	20	70	5	20	70
6	2.5	79	6	2.5	79
7	80	40	7	80	40
8	160	40	8	160	40
9	5	2.5	9	5	2.5
10	5	5	10	5	5
11	5	10	11	5	10
12	5	20	12	5	20
13	5	40	13	5	40
14	5	80	14	5	80
15	1.25	71.25	15	1.25	71.25
16	0.8	71	16	0.8	71
17	5	1.25	17	5	1.25
18	2.5	10	18	2.5	10
19	2.5	40	19	2.5	40
20	2.5	2.5	20	2.5	2.5
21	0.8	1.25	21	0.8	1.25
22	20	1.25	22	20	1.25

Table 5.1: Stanford inductance test chip screening results with different screening input rise times. (a) 50 ps. (b) 150 ps.

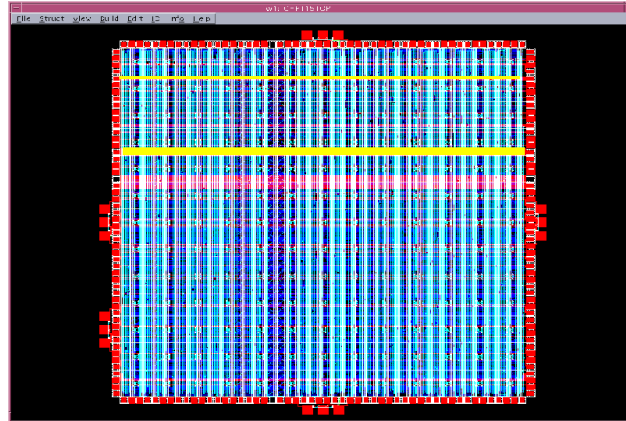
The nets that are selected from the inductance screening tool are highlighted in grey. This test chip was designed to measure the line inductance, so the top layer nets were designed to have a large inductance with different geometries and no devices connected. *Pin rise time* is specified to perform the screening, because no library file is available. The screening is performed for two different rise times, 50 ps and 150 ps with  $\gamma$  of 0.2. With this screening criteria, the screening tool selects nets with a *RC* and *RLC* delay difference larger than 20% of the specified rise time. For a rise time

of 50 ps, all the nets except NET 21 are selected as shown in Table 5.1(a). NET 21 is the narrowest line in the design, so it has the highest resistance. NET 16 is also 0.8  $\mu\text{m}$  wide, so it has the same resistance as NET 21, but the spacing to the ground line is larger. The farther the ground line, the larger the loop size, so NET 16 has a larger inductance than NET 21. Note that 50 ps is an unrealistically fast signal rise time for this technology.

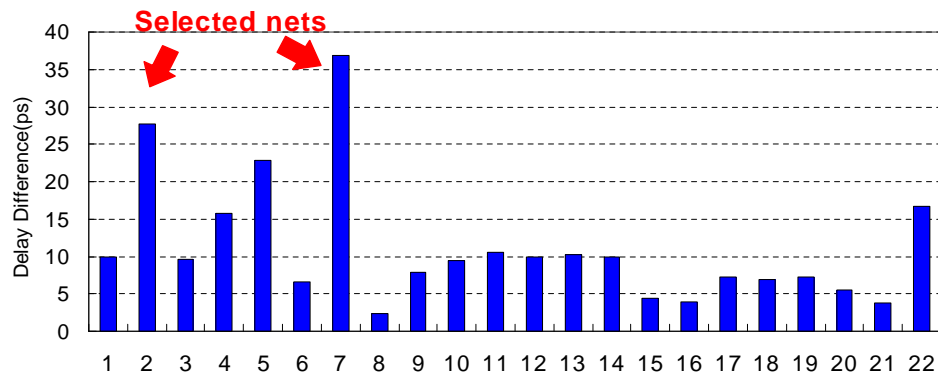
For rise time of 150 ps in Table 5.1(b), only 2 nets are selected. For the inductance effect to be visible even at 150 ps, the line should have a very low resistance. So the selected lines are among the widest lines in the design. However, NET 8 with a 160  $\mu\text{m}$  width is not selected. Because inductance decreases logarithmically as width increases, the inductance value for this net is very low, even though the line resistance is also low. Figure 5.1(a) highlights the selected nets in the layout. Finally, HSPICE simulations are performed for all the nets in the design to verify the screening results. Figure 5.1(b) shows the difference between  $RC$  and  $RLC$  delays with a 150 ps input signal rise time. The two signal lines that have the largest differences are the ones that are selected from the inductance screening tool.

### 5.1.2 Commercial ASIC Designs

Two commercial ASIC designs are tested with the inductance screening tool. The test chips were designed with a 0.13  $\mu\text{m}$  technology, and had a total number of 167,000 and 912,000 nets, respectively. The specifications of the test chips are summarized in Table 5.2. For both designs, when they are tested with their own timing technology library files, no nets are selected to have inductance effects. In order to examine how the inductance effects worsen as rise time decreases, user-input-rise-times are used to



(a)



(b)

Figure 5.1: Stanford inductance test chip screening results and verification for 150 ps rise time. (a) The selected nets are highlighted in the layout. (b)  $RC$  and  $RLC$  delay difference,  $\Delta t_d$ , from HSPICE.

perform screening.

	Design 1	Design 2
Technology	0.13 $\mu$ m, 6ML	0.13 $\mu$ m, 8ML
Chip size (mm $\times$ mm)	4.0 $\times$ 1.3	10.3 $\times$ 10.3
Total # of nets	167K	912K
Total # of cells	166K	692K
SPF file size (MB)	177	808

Table 5.2: Summary of ASIC test examples

In order to see how the results change with the screening criteria, inductance screening is performed for Design 1 and Design 2 for different  $\gamma$ 's and  $t_r$ 's. The results are summarized in Table 5.3.

Criteria		Design 1	Design 2
		(Total # of nets : 167K)	(Total # of nets : 912K)
$\gamma$ ( $t_r$ : 30ps)	0.15	6	328
	0.20	1	98
	0.25	0	4
$t_r$ ( $\gamma$ : 0.20)	20 ps	27	1345
	30 ps	1	98
	40 ps	0	0

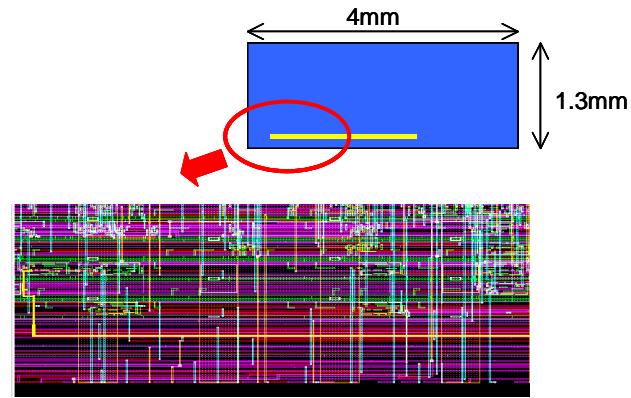
Table 5.3: Number of nets selected with different screening criteria

Usually, around 10% of the total nets are selected in the pre-screening step. More nets are selected for a smaller  $\gamma$ . As rise time becomes smaller, more nets show inductance effects. Even with a very fast input rise time, the actual number of nets selected after the main screening is less than 0.1% of the total nets. These results strongly support the necessity of the screening tool, since inductance is not a problem

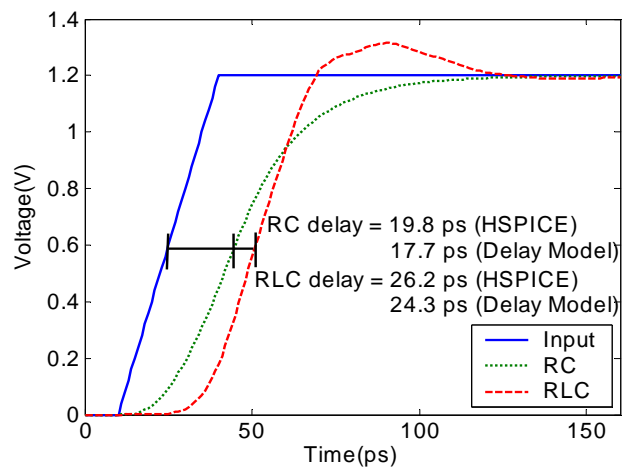
for most of the nets in a design.

For Design 1, with the screening criteria of  $\gamma = 0.2$  and user input rise time of  $t_r = 30$  ps, one net is finally selected. The selected net is a 2 mm global signal line as shown in Figure 5.2(a). The total number of inductors in the original .SPF file before screening was 671,848. The number reduces to 12 after the screening. Therefore, it would be a great waste of resources to extract inductance and include inductance models for all the nets, especially when only a very small portion of them affect the signal integrity. For the selected nets, the tool also reports that the sensitivity of *RLC* delay to inductance is 0.2 for this net. Since the sensitivity is small, no further refinement of inductance extraction with the *4-Return Model* is necessary. HSPICE simulations are performed using *RC* and *RLC* wire models to verify the screening results and test the accuracy of the delay models developed in Chapter 4. The simulated waveform and the delay values are shown in Figure 5.2(b). HSPICE gives  $\Delta t_d$  of 6.4 ps, and delay models predict  $\Delta t_d$  of 6.6 ps.

For Design 2, the length distributions of the selected nets for different  $t_r$ 's and  $\gamma$ 's are examined and they are shown in Figure 5.3. The total net length distribution of the design is also shown for reference. The selected nets have medium lengths, because short wires do not show transmission line effects and very long wires have high signal attenuation. Figure 5.3(a) shows how the distribution changes as  $t_r$  becomes smaller. As rise time gets faster, shorter wires show inductance effects, but the distribution does not spread to longer lines because they have high signal attenuation. The results are in good agreement with the theoretical prediction shown in Chapter 3 [22]. Figure 5.3(b) shows how the distribution changes for different  $\gamma$ 's. Larger  $\gamma$  means less selective screening, the lines selected in larger  $\gamma$  are the wires with more

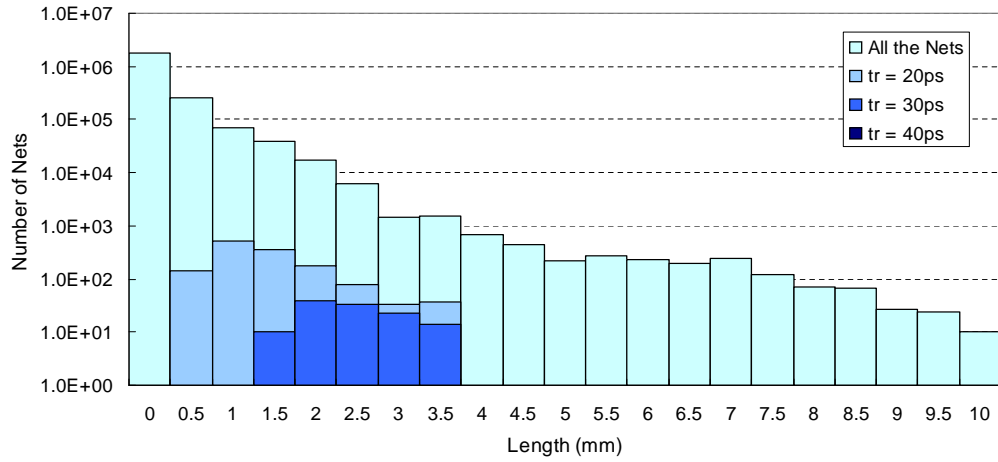


(a)

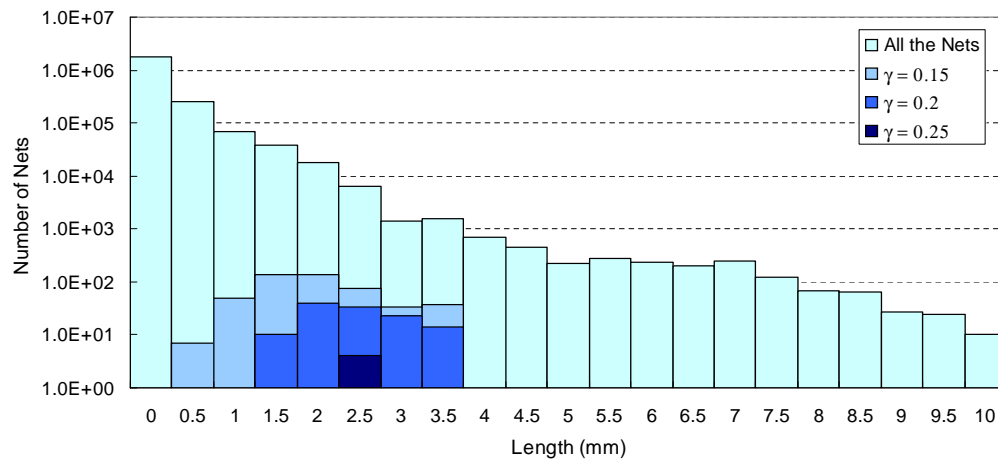


(b)

Figure 5.2: Inductance screening results of Design 1. (a) One global signal line was selected from the inductance screening tool. (b) HSPICE simulation of the selected net in Design 1 with input rise time of 30 ps.



(a)



(b)

Figure 5.3: The range of interconnect lengths where inductance effects are significant for Design 2. (a) Selected net length distribution for different rise times. (b) Selected net length distribution for different  $\gamma$ 's.

severe inductive effects.

## 5.2 Techniques to Reduce Inductance Effects

For the nets selected from the screening, several techniques can be applied to reduce the impact of inductance. Since the significance of an inductance effect is a strong function of signal rise time, one can increase the signal rise time. Based on the delay models proposed in Chapter 4, we derive a criterion on necessary increase in rise time. Since the line inductance can be reduced by modifying the layout on the interconnect, we propose several layout techniques in this section.

### 5.2.1 Increasing Rise Time to Reduce Inductance Effects on Delay

The main screening criteria is based on the difference of  $RC$  and  $RLC$  delays as the following:

$$t_{dRLC}(\zeta, \omega t_r) - t_{dRC}(t_r/\tau) \geq \gamma t_r \quad (5.2)$$

In Chapter 4, it has been shown that if the rise time increases, the  $RC$  delay increases. However, for low loss inductive lines, the  $RLC$  delay decreases as rise time increases, because the inductance effect becomes smaller. Hence, for the selected nets, if the rise time is increased by a certain amount, the delay difference will meet the screening criterion as follows:

$$t_{dRLC}(\zeta, \omega(t_r + \Delta t_r)) - t_{dRC}((t_r + \Delta t_r)/\tau) = \gamma(t_r + \Delta t_r) \quad (5.3)$$

We can find  $\Delta t_r$  based on the delay formulae developed in Chapter 4. The actual delays in terms of dimensionless delays,  $f_{RC}$  and  $f_{RLC}$ , are the following:

$$\begin{aligned} t_{dRC} &= \tau f_{RC}(t_r/\tau) \\ t_{dRLC} &= \frac{1}{\omega} f_{RLC}(\zeta, \omega t_r) \end{aligned} \quad (5.4)$$

Equation 5.3 can be expressed in terms of  $f_{RC}$  and  $f_{RLC}$ .

$$f_{RLC}(\zeta, \omega(t_r + \Delta t_r)) - 2\zeta f_{RC}((t_r + \Delta t_r)/\tau) = \gamma\omega(t_r + \Delta t_r) \quad (5.5)$$

Based on the first order Taylor expansion of non-dimensionalized delay equations,  $\Delta t_r$  can be determined by solving the following:

$$f_{RLC}(\zeta, \omega t_r) + \omega \Delta t_r \cdot \left. \frac{\partial f_{RLC}}{\partial(\omega t_r)} \right|_{\zeta, \omega t_r} - 2\zeta \left[ f_{RC}(t_r/\tau) + \Delta t_r/\tau \cdot \left. \frac{\partial f_{RC}}{\partial(t_r/\tau)} \right|_{t_r/\tau} \right] \approx \gamma\omega(t_r + \Delta t_r) \quad (5.6)$$

The percentage increase in the rise time to reduce inductance effect is the following:

$$\Delta t_r/t_r \approx \frac{f_{RLC} - 2\zeta f_{RC} - \gamma\omega t_r}{2\zeta \frac{t_r}{\tau} \frac{\partial f_{RC}}{\partial(t_r/\tau)} - \omega t_r \frac{\partial f_{RLC}}{\partial(\omega t_r)} + \gamma\omega t_r} \quad (5.7)$$

One signal line is selected from the screening with  $t_r = 30$  ps and  $\gamma = 0.2$  for Design 1 shown in Figure 5.2. For this net, Equation 5.7 gives  $\Delta t_r/t_r$  to be 7.3%. If the rise time increases to 32 ps, the  $RLC$  and  $RC$  delay difference becomes smaller than the screening criterion. This method to reduce the inductance effect is very effective to implement, as it should be straightforward to reduce the driver size to increase the input signal rise time. An added benefit is the slight reduction of peak switching current.

### 5.3 Interconnect Layout Techniques to Reduce Inductance Effects

In this section, we provide some interconnect layout guidelines to reduce on-chip parasitic inductance effects. However, these techniques usually increase the wire capacitance. As a result, once the design is modified, the line characteristics should be carefully evaluated again. If the spacing from the signal line to the current return path is reduced, the current loop size becomes smaller, and hence the inductance becomes smaller. For a signal line with return path only on one side, another return path can be added on the other side to reduce inductance. This approach effectively connects the two inductors in parallel, so the total line inductance decreases.

#### 5.3.1 Dedicated Power and Ground Plane

Figure 5.4 shows the advantage of adding a dedicated power/ground plane to reduce inductance. In Figure 5.4, the coplanar signal line originally has 0.32 nH/mm. By

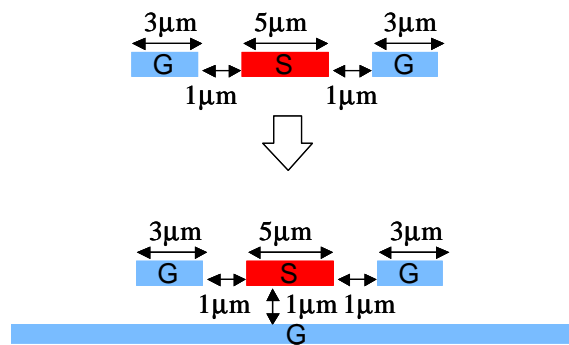


Figure 5.4: Adding a dedicated power/ground plane reduces inductance.

adding the power/ground plane, the inductance value is reduced to 0.20 nH/mm.

However, the capacitance increases from 54 fF/mm to 82 fF/mm. This design technique to dedicate a metal layer as a power/ground plane was applied in Alpha microprocessors [57]. The dedicated plane can always act as a current return path when a power/ground line is not near a signal line, preventing the return path from forming a large current loop. This technique also facilitates the power distribution over the chip.

### 5.3.2 Interdigitating Signal Line

Inductance can be reduced by dividing the wide signal line into narrower lines as shown in Figure 5.5. This technique is called interdigitation, and is popular in designing clock lines to reduce line inductance at the expense of chip area [58, 59].

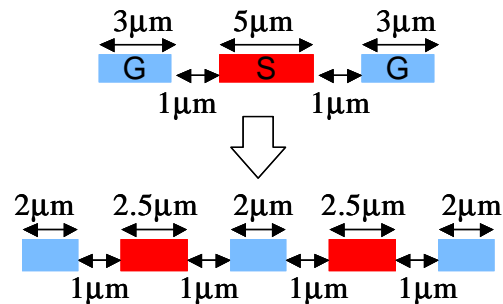


Figure 5.5: Interdigitating the signal lines with power and ground lines reduces inductance.

Figure 5.5 shows a 5 μm wide signal line divided into two 2.5 μm wide lines. This interdigitation divides one inductance loop into two parallel loops, and each line becomes more resistance dominated. The inductance is reduced from 0.32 nH/mm to 0.18 nH/mm. The width of the total line structure increases from 13 μm to 15 μm.

## 5.4 Summary

In this chapter, we present the inductance screening results of three IC designs. The screening results show that less than 0.1% of the nets in a design have inductance problems, supporting the necessity for an inductance screening process. As a result, for future full-chip level inductance extraction, instead of trying to extract the most accurate inductance value for all the nets in a design, it is more efficient to first perform the screening based on rapid self inductance estimation. Subsequently, accurate inductance extraction based on field-solver can be performed on the selected nets. Length distributions for the inductive nets found from the test designs show that there is a range of net lengths where inductance effects are significant and this range is consistent with the theoretical predictions by Ismail [22].

Several techniques are proposed to reduce the inductance effects for the nets that are selected from screening.

# Chapter 6

## Conclusions

### 6.1 Summary

This thesis describes the modeling and screening of on-chip parasitic inductance in digital circuits. As clock frequency increases beyond the GHz range, there has been a grave concern that on-chip parasitic inductance will degrade the signal integrity. In contrast to the resistance and capacitance, it will be infeasible to extract the inductance for all the nets in a design. But no design tool has been available to identify which nets will experience inductance problem.

In Chapter 2, we examine the assumption of current return paths in inductance modeling and develop analytical formulae for the worst case inductance in the presence of multiple return paths. The number of return paths that should be included in the inductance extraction is a complicated function of wire geometry and signal frequency. The window size for accurate inductance extraction is proposed based on  $S$ -parameter and delay simulations using different wire models. It is found that

inductance screening can be performed with no significant error based on the inductance estimated with two closest current return paths. For accurate delay estimation, it may be necessary to include up to two pairs of neighboring current return paths. Full-wave simulation results show that the return current through inter-line capacitors has negligible effect on inductance extraction up to tens of GHz range.

In Chapter 3, a two-step inductance screening algorithm is developed. A stand-alone inductance screening tool is implemented using C language based on standard input file formats. This inductance screening algorithm and tool can be embedded in commercial parasitic extraction and static timing analysis tools.

In Chapter 4, new  $RC$  and  $RLC$  delay models that retain the efficiency and simplicity of the Elmore delay are developed to perform inductance screening. The proposed parameterized delay models accurately predict the delays as a function of input rise time and wire parameters. In addition, from the parameterized delay models, we can derive the sensitivity of  $RLC$  delay to inductance. It is found that the  $RLC$  delay is less sensitive to inductance than to resistance and capacitance. To further improve the accuracy of the delay model, a new correction method,  $EDCF$ , is proposed to consider resistive shielding of downstream capacitance.  $EDCF$  is derived by comparing the signal propagation in a distributed  $RC$  transmission line and Elmore's approximation of a single line structure. This concept is generalized to tree structured nets.  $EDCF$  can be used to correct the delays for both  $RC$  and  $RLC$  tree structures.

The inductance screening results of real IC designs are shown in Chapter 5. It is confirmed that only a small percentage of the nets show inductance effects, supporting the necessity of an inductance screening process. The distributions of net length

indicate that there is a range of lengths where inductance effects are significant.

The approaches and guidelines presented in this thesis will enable full-chip inductance screening and extraction for future CAD tools. Inductance screening is performed based on the inductance estimated with two neighboring returns, which can be implemented with no additional overhead on the existing extraction engine. For the selected nets whose delays are very sensitive to the inductance, more accurate inductance extraction can be performed with up to four neighboring returns.

## 6.2 Future Work

The crosstalk noise due to mutual inductance is a potential problem in signal integrity. Since inductive crosstalk is not likely to occur among very resistive or very short wires [21], the screening algorithm developed in this work can also be applied to select the nets that may be prone to inductive crosstalk. If the inductance screening is performed with a reasonable criteria, less than 10% of the total nets will be selected. Then, among those selected nets, further detailed criteria can be developed to determine the sensitivity of the crosstalk, based on the current loop sizes and the distances between loops.

In this thesis, we proposed *EDCF* based on the generalization of a uniformly distributed single line analysis to a tree structured net. The capacitive loading at the fanouts of a tree can affect the modeling of *EDCF* as well. In order to improve the accuracy, we can consider linear or higher order variation in the resistance and capacitance of the single line analysis to better represent a specific tree structure.

# Appendix A

## Derivation of the $RC$ and $RLC$ Delay Models

### A.1 RC Delay Model

For slow input shown in Figure 4.5 (b), the output waveform reaches the 50% delay point before the ramp input reaches  $V_{dd}$  ( $\bar{v}_{out}(t_r/\tau) \geq 0.5$  or  $t_r/\tau \geq 1.6$ ). Even though the waveform has an analytic expression with respect to  $\bar{t}$ ,  $\bar{t}_d$  cannot be solved analytically. From the numerical solutions, the fitting function for  $f_{RC}(t_r/\tau)$  is chosen as the following:

$$f_{RC}(t_r/\tau) = 1 - \exp\left(-a(t_r/\tau)^b\right) \quad (\text{A.1})$$

Since the expression is not linear with respect to  $a$  and  $b$ , the fitting parameters are found by solving an optimization problem with the Nelder-Mead non-linear simplex method [34]. We need to find  $a$  and  $b$  that minimize  $J$  for the given  $n$  number of data

points as the following:

$$x_i \geq 1.6 \quad (1 \leq i \leq n) \quad (\text{A.2})$$

$$y_i = f_{RC}(x_i)$$

$$J = \sum_{i=1}^n \left[ y_i - \left( 1 - \exp(-ax_i^b) \right) \right]^2 \quad (\text{A.3})$$

The optimizer gives  $a = 1.136$  and  $b = 0.6933$ , so the dimensionless delay in this region is the following:

$$f_{RC}\left(\frac{t_r}{\tau}\right) \approx 1 - \exp[-1.136(t_r/\tau)^{0.6933}] \quad (\text{A.4})$$

## A.2 RLC Delay Model

When  $0 \leq \zeta \leq 1.3$  and  $0 \leq \omega t_r \leq 10$ , for a fixed  $\omega t_r$ , we can approximate the delay with a straight line.

$$\bar{t}_d \cong a_1 \zeta + a_0 \quad (\text{A.5})$$

For  $n$  data points, Equation A.5 can be expressed in a matrix form as the following:

$$A \begin{bmatrix} a_1 \\ a_0 \end{bmatrix} = b \quad (\text{A.6})$$

where

$$A = \begin{bmatrix} \zeta_1 & 1 \\ \zeta_2 & 1 \\ \vdots & \vdots \\ \zeta_n & 1 \end{bmatrix}, b = \begin{bmatrix} \bar{t}_{d1} \\ \bar{t}_{d2} \\ \vdots \\ \bar{t}_{dn} \end{bmatrix} \quad (\text{A.7})$$

Using the least square method,  $a_1$  and  $a_0$  are calculated from the following:

$$\begin{bmatrix} a_1 \\ a_0 \end{bmatrix} = (A^T A)^{-1} A^T b \quad (\text{A.8})$$

The procedure can be repeated for different  $\omega t_r$ 's, as  $a_1$  and  $a_0$  change with respect to  $\omega t_r$ .

$$a_j(\omega t_r) = a_{j3}(\omega t_r)^3 + a_{j2}(\omega t_r)^2 + a_{j1}(\omega t_r) + a_{j0}, \quad j = 0, 1 \quad (\text{A.9})$$

$$A = \begin{bmatrix} (\omega t_r)_1^3 & (\omega t_r)_1^2 & (\omega t_r)_1 & 1 \\ (\omega t_r)_2^3 & (\omega t_r)_2^2 & (\omega t_r)_2 & 1 \\ \vdots & \vdots & \vdots & \vdots \\ (\omega t_r)_n^3 & (\omega t_r)_n^2 & (\omega t_r)_n & 1 \end{bmatrix}, \quad b_j = \begin{bmatrix} a_j((\omega t_r)_1) \\ a_j((\omega t_r)_2) \\ \vdots \\ a_j((\omega t_r)_n) \end{bmatrix} \quad (\text{A.10})$$

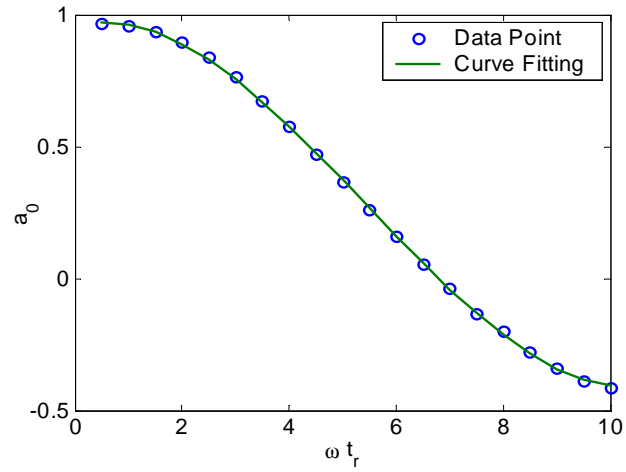
From the data points found from Equation A.8 for different  $\omega t_r$ 's, we can use the least square method to find  $a_{j0}$ ,  $a_{j1}$ ,  $a_{j2}$ , and  $a_{j3}$ .

$$\begin{bmatrix} a_{j3} \\ a_{j2} \\ a_{j1} \\ a_{j0} \end{bmatrix} = (A^T A)^{-1} A^T b_j, \quad j = 1, 2 \quad (\text{A.11})$$

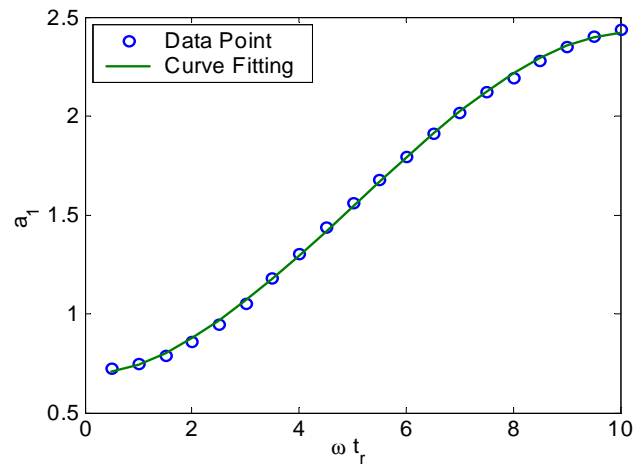
The results are the following:

$$\begin{aligned} a_1(\omega t_r) &= -0.003(\omega t_r)^3 + 0.047(\omega t_r)^2 + 0.014(\omega t_r) + 0.69 \\ a_0(\omega t_r) &= 0.003(\omega t_r)^3 - 0.048(\omega t_r)^2 + 0.051(\omega t_r) + 0.96. \end{aligned} \quad (\text{A.12})$$

Figure A.1 shows how the curve-fitted coefficients match the numerical solutions.



(a)



(b)

Figure A.1: Coefficients that characterize *RLC* delay (a)  $a_0(\omega t_r)$ , and (b)  $a_1(\omega t_r)$ .

# Appendix B

## Derivation of EDCF

We can find the approximated algebraic expression for *EDCF* as a function of  $t_r/RC$  and  $x/l$ . From the numerical solutions, when  $x/l \leq 0.6$ , for a fixed  $t_r/RC$ , the expression for *EDCF* is approximated to a second-order polynomial of  $x/l$ .

$$\text{EDCF}(\bar{x}) = \frac{t_{dElmore} - t_{dDiffusion}}{t_{dDiffusion}} \cong c_2\bar{x}^2 + c_1\bar{x} + c_0 \quad (\text{B.1})$$

where  $\bar{x} = x/l$ .

The fitting parameters,  $c_0$ ,  $c_1$ , and  $c_2$  are functions of  $t_r/RC$  and they can be found from the least square method as the following:

$$A \begin{bmatrix} c_2 \\ c_1 \\ c_0 \end{bmatrix} = b \quad (\text{B.2})$$

where

$$A = \begin{bmatrix} \bar{x}_1^2 & \bar{x}_1 & 1 \\ \bar{x}_2^2 & \bar{x}_2 & 1 \\ \vdots & \vdots & \vdots \\ \bar{x}_n^2 & \bar{x}_n & 1 \end{bmatrix}, \quad b = \begin{bmatrix} EDCF(\bar{x}_1) \\ EDCF(\bar{x}_2) \\ \vdots \\ EDCF(\bar{x}_n) \end{bmatrix} \quad (\text{B.3})$$

Then the coefficients can be found from the following:

$$\begin{bmatrix} c_2 \\ c_1 \\ c_0 \end{bmatrix} = (A^T A)^{-1} A^T b \quad (\text{B.4})$$

From the trend of the coefficients found from Equation B.4, the fitting function for each coefficients is decided as the following:

$$c_j(t_r/RC) \cong p_j \exp[-q_j(t_r/RC)] + r_j, \quad j = 0, 1, 2 \quad (\text{B.5})$$

Since the expression is not linear with respect to  $p_j$ ,  $q_j$  and  $r_j$ , these fitting parameters are found by solving an optimization problem with a non-linear simplex method as is done for the  $RC$  delay derivation.

After running the optimizer, the coefficients are found, and the expressions for  $c_0$ ,  $c_1$ , and  $c_2$  are as follows:

$$\begin{aligned} c_2(t_r/RC) &= 9.82e^{-3.39t_r/RC} - 0.02 \\ c_1(t_r/RC) &= -11.17e^{-3.15t_r/RC} - 0.16 \\ c_0(t_r/RC) &= 3.21e^{-2.92t_r/RC} + 0.12 \end{aligned} \quad (\text{B.6})$$

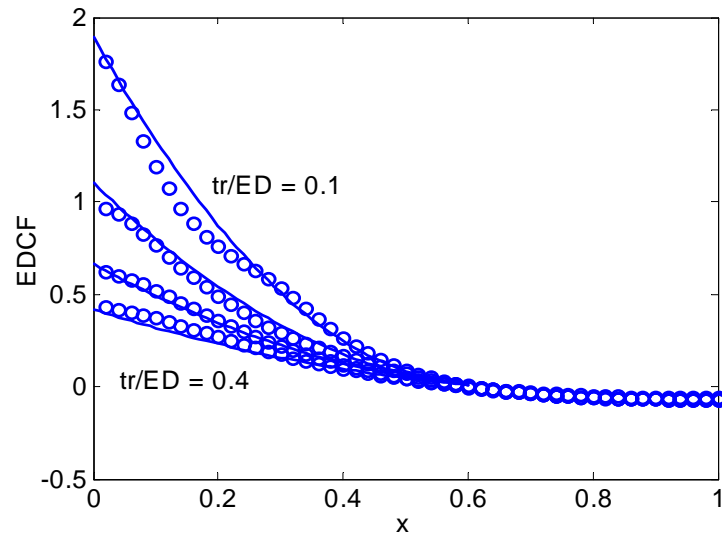


Figure B.1: The matching of the coefficients for the *Effective Distance Correction Factor (EDCF)*.

Figure B.1 shows how the *EDCF* calculated from the curve-fitted coefficients matches the numerical solutions.

# Bibliography

- [1] C. Ryu. Microstructure and reliability of copper interconnects. *Ph.D. thesis*, Stanford University, 1998.
- [2] International technology roadmap for semiconductors (ITRS). 2003.
- [3] Ansoft Corporation. *Maxwell 2D/3D Parameter Extractor*.
- [4] Synopsys Inc. *Raphael 2D and 3D Field Solver*.
- [5] Synopsys Inc. *Star-RC XT Option User Guide*.
- [6] Cadence Design Systems Inc. *Fire and Ice QX*.
- [7] Mentor Graphics Corp. *Calibre xRC*.
- [8] A. Ruehli. Inductance calculations in a complex integrated circuit environment. *IBM Journal of Research and Development*, 16:470–481, September 1972.
- [9] K. Gala, V. Zolotov, R. Panda, B. Young, J. Wang, and D. Blaauw. On-chip inductance modeling and analysis. *Proceedings of 37th Design Automation Conference*, pages 63–68, June 2000.
- [10] M. W. Beattie and L. T. Pileggi. Inductance 101: Modeling and extraction. *Proceedings of 38th Design Automation Conference*, June 2001.

- [11] K. L. Shepard and Zhong Tian. Return-limited inductances: A practical approach to on-chip inductance extraction. *IEEE Transactions on Computer-Aided Design*, 19(4):425–436, April 2000.
- [12] A. Devgan, H. Ji, and W. Dai. How to efficiently capture on-chip inductance effects: Introducing a new circuit element K. *International Conference on Computer-Aided Design*, pages 150–155, 2000.
- [13] W. C. Elmore. The transient response of damped linear networks with particular regard to wideband amplifiers. *Journal of Applied Physics*, 19(1):55–63, January 1948.
- [14] Y. I. Ismail, E. G. Friedman, and J. L. Neves. Equivalent elmore delay for RLC trees. *IEEE Transactions on Computer-Aided Design*, 19(1):83–97, January 2000.
- [15] A. B. Kahng and S. Muddu. An analytical delay model for RLC interconnects. *IEEE Transactions on Computer-Aided Design*, 16(12):1507–1514, December 1997.
- [16] K. Agarwal, D. Sylvester, and D. Blaauw. An effective capacitance based driver output model for on-chip RLC interconnects. *Proceedings of 40th Design Automation Conference*, June 2003.
- [17] R. Gupta, B. Krauter, B. Tutuiianu, J. Willis, and L. T. Pileggi. The Elmore delay as a bound for RC trees with generalized input signals. *Proceedings of 32nd Design Automation Conference*, 1995.

- [18] C. V. Kashyap, C. J. Alpert, and A. Devgan. An effective capacitance based delay metric for RC interconnect. *International Conference on Computer-Aided Design*, pages 229–234, November 2000.
- [19] A. B. Kahng, K. Masuko, and S. Muddu. Analytical delay models for VLSI interconnects under ramp input. *International Conference on Computer-Aided Design*, pages 30–36, November 1996.
- [20] L. T. Pillage and R. A. Rohrer. Asymptotic waveform evaluation for timing analysis. *IEEE Transactions on Computer-Aided Design*, 9(4):352–366, April 1990.
- [21] A. Deutsch *et al.* When are transmission-line effects important for on-chip interconnections? *IEEE Transactions on Microwave Theory and Techniques*, 45(10):1836–1846, October 1997.
- [22] Y. I. Ismail, E. G. Friedman, and J. L. Neves. Figures of merit to characterize the importance of on-chip inductance. *Proceedings of 35th Design Automation Conference*, pages 560–565, June 1998.
- [23] U. S. Inan and A. S. Inan. *Engineering Electromagnetics*, Addison-Wesley, 1999.
- [24] W. J. Dally and J. W. Poulton. *Digital Systems Engineering*, Cambridge University Press, 1998.
- [25] T. Dhaene and D. E. Zutter. Selection of lumped element models for coupled lossy transmission lines. *IEEE Transactions on Computer-Aided Design*, 11(7):805–815, July 1992.

- [26] S. Kim, Y. Massoud, and S. S. Wong. On the accuracy of return path assumption for loop inductance extraction for  $0.1\mu\text{m}$  technology and beyond. *International Symposium on Quality Electronic Design*, pages 401–404, March 2003.
- [27] C.-K. Cheng, J. Lillis, S. Lin, and N. Chang. *Interconnect Analysis and Synthesis*, John Wiley and Sons, 2000.
- [28] F. W. Grover. *Inductance Calculations*, Dover Publications Inc., 1973.
- [29] Ansoft Corporation. *Ansoft HFSS*.
- [30] M. Kamon, M. J. Tsuk, and J. White. FASTHENRY, A Multipole-Accelerated 3-D inductance extraction program. *Proceedings of 30th Design Automation Conference*, June 1993.
- [31] X. Qi, B. Kleveland, Z. Yu, S. Wong, R. Dutton, and T. Young. On-chip inductance modeling of VLSI interconnects. *International Solid-State Circuits Conference*, pages 172–173, December 2000.
- [32] L. He, N. Chang, S. Lin, and O. S. Nakagawa. An efficient inductance modeling for on-chip interconnects. *Custom Integrated Circuits Conference*, May 1999.
- [33] B. Krauter and S. Mehrotra. Layout based frequency dependent inductance and resistance extraction for on-chip interconnect timing analysis. *Proceedings of 35th Design Automation Conference*, pages 303–308, 1998.
- [34] J.A. Nelder and R. Mead. A simplex method for function minimization. *The Computer Journal*, 7(4):308–313, July 1965.

- [35] G. T. Daryanani and J. A. Resh. Foster-distributed-lumped network synthesis. *IEEE Transactions on Circuit Theory*, CT-16(4):429–434, November 1969.
- [36] S.-P. Sim *et al.* An effective loop inductance model for general non-orthogonal interconnect with random capacitive coupling. *International Electronics Devices Meeting*, pages 315–318, December 2002.
- [37] S. Lin, N. Chang, and S. Nakagawa. Quick on-chip self- and mutual-inductance screen. *International Symposium on Quality Electronic Design*, pages 513–520, March 2000.
- [38] P. Zarkesh-Ha, J. A. Davis, and J. D. Meindl. Prediction of net-length distribution for global interconnects in a heterogeneous system-on-a-chip. *IEEE Transactions on VLSI Systems*, 8(6):649–659, December 2000.
- [39] J. W. Nilson. Electric circuits. *Addison-Wesley Publishing Company*, May 1993.
- [40] A. Deutsch *et al.* Frequency-dependent crosstalk simulation for on-chip interconnections. *IEEE Transactions on Advanced Packaging*, 22(3):292–308, August 1999.
- [41] Y. Massoud, J. Kawa, D. MacMillen, and J. White. Modeling and analysis of differential signaling for minimizing inductive cross-talk. *Proceedings of 38th Design Automation Conference*, June 2001.
- [42] H. H. Chen and J. S. Neely. Interconnect and circuit modeling techniques for full-chip power supply noise analysis. *IEEE Transactions on Components, Packaging and Manufacturing Technology*, 21(3):209–215, August 1998.

- [43] L.-R. Zheng and H. Tenhunen. Fast modeling of core switching noise on distributed LRC power grid in ULSI circuits. *IEEE Transactions on Advanced Packaging*, 24(3):245–254, August 2001.
- [44] B. Kleveland. CMOS interconnects beyond 10 GHz. *Ph.D. thesis*, Stanford University, 2000.
- [45] H. B. Bakoglu. Circuits, interconnections and packaging for VLSI. *Addison-Wesley Publishing Company*, September 1989.
- [46] T. H. Cormen, C. E. Leiserson, R. L. Rivest, and C. Stein. Introduction to algorithms. *MIT Press 2nd Edition*, September 2001.
- [47] L. T. Pileggi. Timing metrics for physical design of deep submicron technologies. *Proceedings of International Symposium on Physical Design*, 1998.
- [48] R. Gupta, B. Tutuianu, and L. T. Pileggi. The Elmore delay as a bound for RC trees with generalized input signals. *IEEE Transactions on Computer-Aided Design*, 16(1):95–104, January 1997.
- [49] C. J. Alpert, A. Devgan, and C. V. Kashyap. RC delay metrics for performance optimization. *IEEE Transactions on Computer-Aided Design*, 20(5):571–582, May 2001.
- [50] J.L. Wyatt. Circuit analysis, simulation and design. *Elsevier Science Publishers*, North-Holland, 1987.
- [51] J. Rubinstein, P. Penfield, and M. Horowitz. Signal delay in RC tree networks. *IEEE Transactions on Computer-Aided Design*, CAD-2(3):202–211, July 1983.

- [52] C. L. Ratzlaff, N. Gopal, and L. T. Pillage. RICE: Rapid interconnect circuit evaluator. *IEEE Transactions on Computer-Aided Design*, 13(6):763–776, June 1994.
- [53] R. Kay and L. T. Pileggi. PRIMO: Probability interpretation of moments for delay calculation. *Proceedings of 35th Design Automation Conference*, 1998.
- [54] C. V. Kashyap, C. J. Alpert, F. Liu, and A. Devgan. Closed form expressions for extending step delay and slew metrics to ramp inputs. *The International Symposium on Physical Design*, 2003.
- [55] J. D. Anderson Jr. *Fundamentals of Aerodynamics*, McGraw Hill, 1991.
- [56] R. L. Liboff. *Introductory Quantum Mechanics*, Addison-Wesley Publishing Company, 1992.
- [57] B. J. Benschneider *et al.* A 1GHz Alpha microprocessor. *International Solid-State Circuits Conference*, pages 86–87, February 2000.
- [58] Y. Massoud, S. Majors, T. Bustani, and J. White. Layout techniques for minimizing on-chip interconnect self inductance. *Proceedings of 35th Design Automation Conference*, pages 566–571, 1998.
- [59] X. Huang, P. Restle, T. Bucelot, Y. Cao, and T.-J. King. Loop-based interconnect modeling and optimization approach for multi-GHz clock network design. *Custom Integrated Circuits Conference*, pages 19–22, 2002.